Design of a RF Transmitter for RFID Tags in a New Technology with Ultra Thin Silicon Substrates

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***Abstract*—A test-chip for exploring the possibility of implementing RFID on a new 0.5-μm gate-array technology, with 20-μm Si substrates, is presented. It comprises of 4 transmitter circuits based on two ring oscillators and two cross-coupled oscillators. The design strategy adopted ensures simplicity in circuit design and a wide tuning range to account for the uncertainty implicated by the new technology. One cross-coupled VCO operates at 2.45 GHz in the ISM band with a 35% tuning ratio. It features a 4-band frequency tuning characteristic utilizing a binary-weighted switched capacitor bank and MOS varactors. Power consumption of the VCO core is 23 mW with a tail current of 5 mA.**

***Index Terms*—Analog integrated circuit, CMOS, HF transmitters, LC oscillators, RFID, voltage controlled oscillator (VCO).**

I. Introduction

Radio frequency identification (RFID) is a powerful and promising technology. As such, cheap solutions for its implementation are constantly being investigated. It is also imperative to develop small and flexible RFID chips allowing them to be placed in price tags, ID cards, and even in humans or animals. A new CMOS technology of ultra-thin silicon substrates (20-μm) and 0.5-μm sea-of-gates technology provide these opportunities for development. In this work, the implementation of RF transmitter circuits on a digital gate array employing this new technology is investigated.

In order to fully examine the possibility of RFID implementation, it is the first step to test various transmitter structures using the new technology. For this purpose, simple architectures are chosen for the first prototypes, which have wide tuning ranges as well to ensure that any uncertainties are compensated for. It is also important to have a variety in terms of transmitter topologies, operating frequencies and tuning methods so that a meaningful test-chip is created on which these parameters could be effectively compared and optimized.

A prefabricated chip with a sea-of-gates structure is used for prototyping. Four transmitters are designed on the single chip. The transmitters consist of two cross-coupled voltage controlled oscillators (VCO) and two ring VCOs. The cross-coupled oscillators are identical with the components scaled for the two frequencies of 2.45 GHz (ISM band) and 869 MHz (SRD-Band). The ring oscillators are both CMOS-based implementations, one of them is single-ended while the other one is differential.

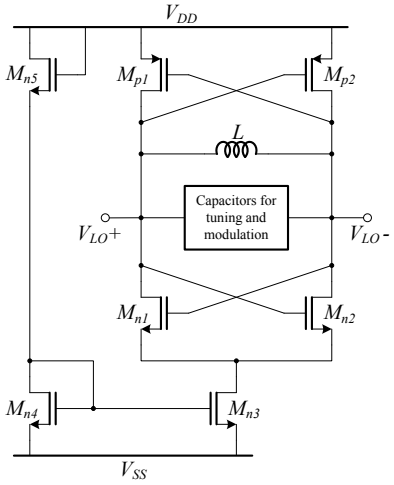

Fig. 1. Basic schematic of cross-coupled oscillators.

II. Cross-Coupled VCO Design

Cross-coupled VCOs operate on the principle of LC resonance. Once energy is injected into an LC resonator it should oscillate at the natural frequency of the system $f = \frac{1}{2\pi\sqrt{LC}}$ and maintain oscillation indefinitely. However, due to the presence of parasitic losses, this energy is gradually dissipated and oscillation discontinues. To compensate for these losses an active circuit is added to sustain oscillation.

The basic structure of the cross-coupled VCO is shown in fig. 1. It consists of an LC resonant circuit, negative transconductance components using both NMOS ($M_{n\{1,2\}}$) and PMOS ($M_{p\{1,2\}}$) transistors, a current generation branch ($M_{n\{4,5\}}$) and a current mirroring transistor (M_{n3}). The negative transconductance components are responsible for compensation of the resonant tank's losses by having an equivalent negative resistance ($R = -\frac{2}{g_m}, g_m$ is the transconductance of the transistors) [1] designed to cancel out the LC tank's parasitic resistance.

A. Analog Frequency Tune

Continuous frequency variation is done through a varactor diode. This is realized using the new technology by connecting

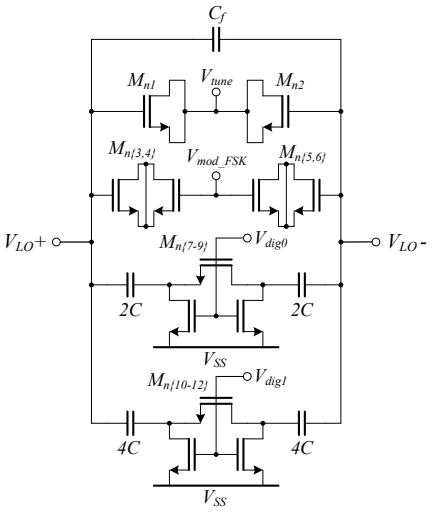

Fig. 2. Proposed capacitor bank used for frequency tuning and modulation.

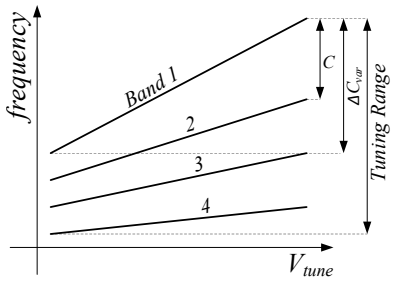

Fig. 3. Tuning characteristic of a 2 bit capacitor bank.

together the source and drain of a MOS transistor making it a two terminal device ($M_{n\{1,2\}}$ in fig. 2). The capacitance of this component consists of the oxide capacitance, which is fixed, plus the depletion capacitance which is proportional to the voltage drop across the device terminals [2].

B. Discrete Frequency Tune

The use of pass-gate logic allows the switching-on or off of capacitors thereby resulting in discrete changes of frequency. It can be seen in fig. 2 that two such *switched* capacitors are used and it results in a 4-band tuning characteristic. In order to have a uniform change of frequency between each of the frequency bands, the capacitors are binary weighted such that when the digital tune values V_{dig0} and V_{dig1} are 00 the bank capacitance is equal to 0, when it is 01 the capacitance is equal to C, 10 $\rightarrow$ $2C$, and 11 $\rightarrow$ 3C. Additionally, the frequency is continuously tuned within each frequency band by the utilization of varactors. Use of the described discrete frequency variation has the following advantages [3]:

- Increases tuning range.
- Avoids frequency instability and sensitivity to input noise since it lowers the tuning sensitivity (K_{VCO}).
- Lowers power consumption.
- Improves phase noise.

The MOS switches are designed with reduced power dissipation in mind. For that reason, only one pass-transistor is used

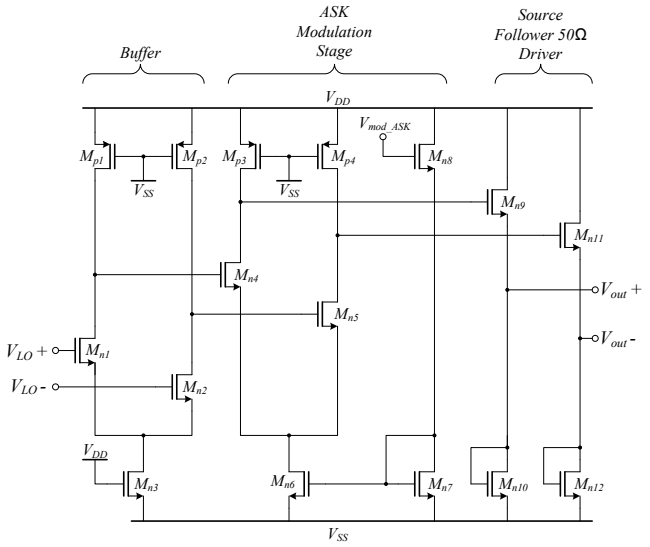

Fig. 4. Proposed differential ASK modulation and output stage used in the cross-coupled oscillators and the differential ring oscillator.

for switching, and the structure is made symmetric by using two capacitors, which have lesser parasitic losses, as shown in fig. 2. Placement between the capacitors moves the transistor parasitics away from the oscillation nodes thus improving the resonator quality factor (Q). The transistors connected to VSS at the switch transistor's source and drain ensure correct operation, since the nodes are otherwise floating.

The plot in fig. 3 clarifies the 4 frequency bands resulting from the capacitor bank. It can be observed that K_{VCO} decreases when more capacitors are appended since the variable varactor capacitance (ΔC_{var}) becomes a smaller fraction of the total capacitance. As shown in the figure, the overlap between the frequency bands is controlled by varying C, while the tuning range within each band is controlled by the varactor's ΔC_{var} [3].

C. Frequency Shift Keying (FSK) Modulation

FSK modulation is a variant of digital modulation in which the digital "0" and "1" are each assigned a frequency at a small offset from one another. This can be done by controlling the voltage on the analog tune control, however this has the drawback of high error-rate due to noise sensitivity and small frequency offset required for modulation. This problem is circumvented, as it can be seen from fig. 2, by using a small varactor dedicated for digital modulation input [4], [5]. Placing two small varactors back-to-back means that the variable capacitance is halved due to the series combination, which lowers the frequency offset to the required value of $\pm$100 kHz.

D. Buffer, Amplitude Shift Keying (ASK) Modulation Stage and Output Driver

The output stage is designed to drive a 50 Ω load, which is also the termination of most measurement equipment. A buffer with small input transistors is placed to isolate the local

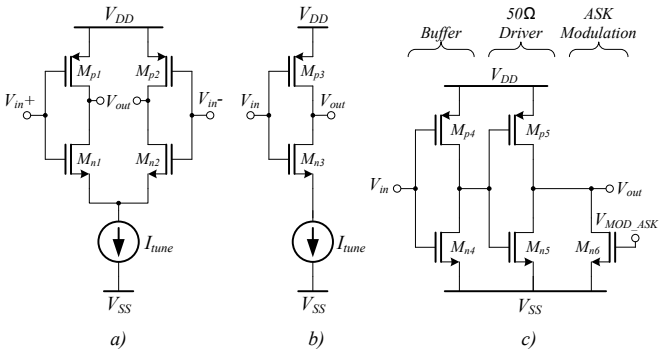

Fig. 5. A CMOS a) differential and b) single-ended inverter. c) CMOS output stage used in the single-ended ring oscillator.

oscillator (LO) signal and avoid frequency pulling. Optional ASK modulation is possible by varying the current through a current mode logic (CML) amplifier as shown in fig. 4. This is followed by a source follower with large transistors to provide enough current and a peak-to-peak voltage of at least 1 V for the 50 Ω load.

III. Ring VCO Design

CMOS configuration is preferred to other common-source or CML topologies since it has lower power consumption and maintains the amplitude of oscillation very well across a wide range of frequencies when tuned through the tail current (I_{SS} in fig. 5). Using this method of tune, the frequency is tuned virtually from DC up to the maximum ring frequency [6].

For the differential ring oscillator the same output stage in fig. 4 is used. As for the single-ended one, a CMOS output stage is designed with the same basic components. A small CMOS inverter is used to buffer the oscillator from the driver and load. This is followed by another inverter with larger transistors to provide enough current for the 50 Ω termination. ASK modulation is done simply by connecting a pull-to-ground transistor at the output. It is sized with respect to the driver inverter in order to control the output amplitude with modulation ratio 1:3.

IV. Simulation Results

A. Cross-Coupled VCOs

The plot in fig. 6 shows the frequency tuning characteristic for the 2.45 GHz cross-coupled VCO. The four tuning curves are a result of the possible switching of the 2-bit capacitor bank array, and since there are two branches, there are $2^2 = 4$ possible tune values. A frequency tuning ratio of about 35% is achieved, from 2.05 GHz up to 2.90 GHz. The K_{VCO} for each tuning band increases when moving from a lower band to a higher one with an overall K_{VCO} of 125 MHz/V. Although the tuning linearity is poor across the whole voltage range, it improves greatly if a smaller voltage range ($1.3V - 3.4V$) is chosen. Similar results are obtained for the 900 MHz VCO.

Fig. 7 shows the variation of the LO waveform amplitude across the four frequency bands. It is observed that the amplitude decreases with the frequency, this change in amplitude

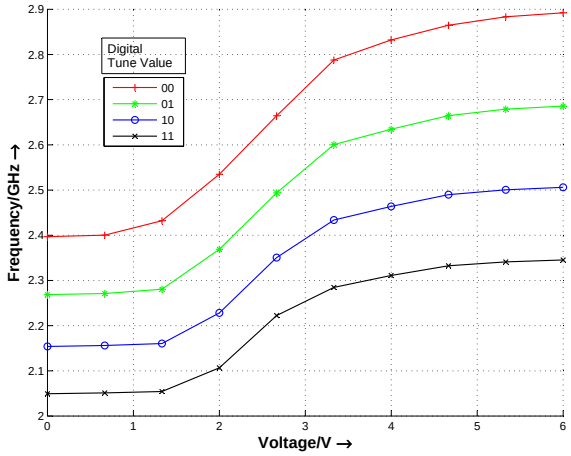

Fig. 6. Frequency tuning characteristic for the 2.45 GHz cross-coupled VCO.

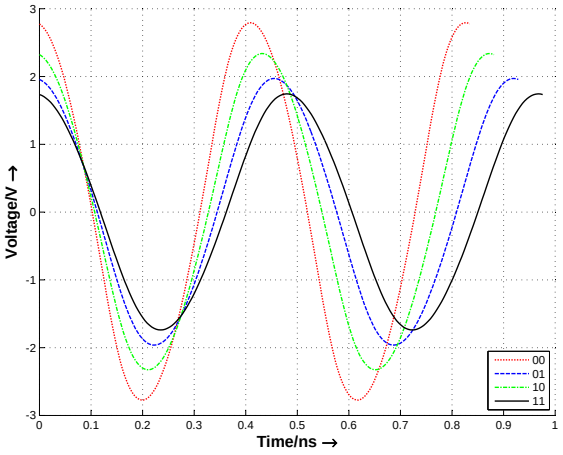

Fig. 7. Local oscillator waveform across different digital tune values for the 2.45 GHz cross-coupled VCO.

can be explained by the extra losses introduced by turning on more of the non-ideal MOS switches [3].

The power consumption of the2.45 GHz VCO is 23 mW with a tail current of 5 mA. The output stage consumes 34 mW of power and the transmitter is able to deliver about 100 mW to a 50 Ω load. For the 900 MHz VCO larger transistors were used in realizing a larger negative transconductance component. This is to compensate for the greater losses found at the lower frequency used, since the passive components have lower Qs at lower frequencies. For this reason the power consumption for the 900 MHz VCO core is higher: 60 mW at 15 mA tail current.

The spectral purity of the cross-coupled VCOs is very good when compared to the ring VCOs. The nearest harmonic distortion component is only about -30 dBm as shown in fig. 8, while that value is greater than zero for both ring VCOs. The phase noise is simulated at -65 dBc/Hz at an offset frequency of 100 kHz.

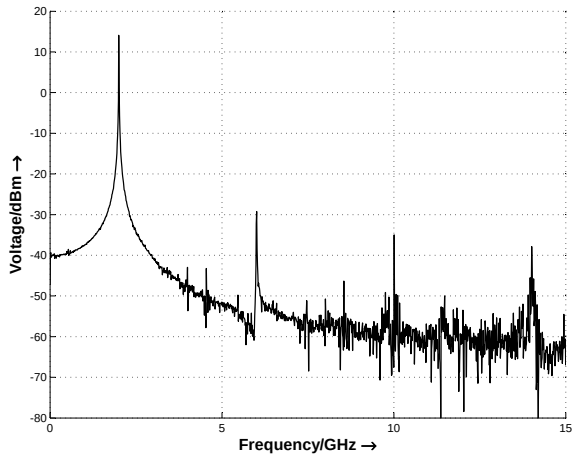

Fig. 8. Frequency spectrum of the 2.45 GHz cross-coupled VCO.

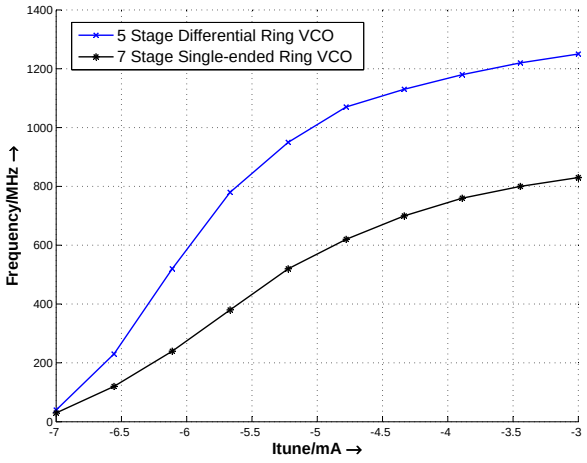

Fig. 9. Frequency tuning characteristic for the ring oscillators.

B. Ring VCOs

The tuning characteristic of the ring VCOs are shown in fig. 9. Ring VCOs, by means of current steering, have wide tuning ranges starting from less than 10 MHz up to 930 MHz and 1.22 GHz for the single-ended and differential ring VCOs respectively. K_{VCO} is quite high due to the large frequency tuning ranges with values of 210 MHz/mA and 325 MHz/mA for the two VCOs.

Power consumption is lower in the single-ended implementation. The VCO consumes only 7 mW compared to 17 mW in the differential one. The single-ended CMOS output stage is however more power hungry: it requires 45 mW which is 9 mW more than the differential CML output stage, and delivers only 25 mW to a 50 Ω load.

V. Layout Considerations

The chip layout is optimized for testing by making output pads of the same type on the same side of the chip. This speeds up testing on a wafer prober since the probes can be relocated quickly between transmitters.

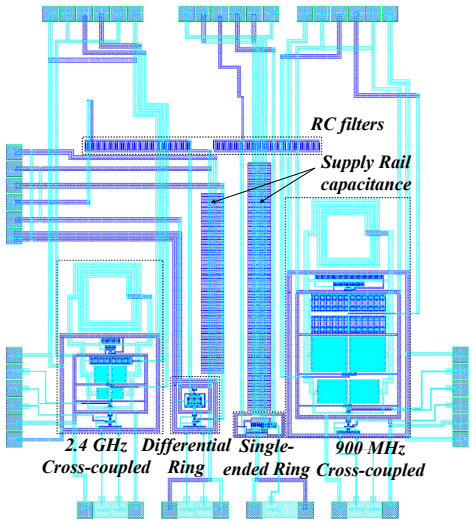

Fig. 10. Layout of the complete PROMIKRON testchip.

Layout of the differential transmitters is designed to be symmetrical to avoid signal skewing. For the purpose of matching in the cross-coupled transistors, the two transistors are split into fingers which are interleaved together to reduce mismatch offsets. In addition, noise filters are placed on the tuning inputs and the supply rail as labeled on fig. 10.

VI. Conclusion

A test-chip consisting of four transmitter circuits was implemented on a 0.5-μm gate-array technology to investigate how RFID tags could be realized using the technology. The proposed transmitters feature simple designs with direct baseband modulation through varactors or ASK modulation by use of current steering. Frequency tuning was implemented in both discrete and continuous form to achieve tuning ratios of at least 35%. With a 5 V supply, power consumption of the VCOs varied from 7 mW up to 60 mW. Based on the simulation results presented, it is concluded that both cross-coupled and ring VCOs can be implemented on the mentioned technology.

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