2.2 GHz LC VCO for RFID on a 0.5-μm digital gate-array designed for ultra-thin silicon substrates

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***Abstract*—A new technology provides opportunities in the implementation of radio frequency identification (RFID) tags. A test chip comprising four transmitter circuits is implemented on a 0.5-μm gate array designed for flexible ultra-thin silicon substrates (20 μm). Two transmitters are based on the cross-coupled oscillator topology and two are based on ring oscillators. The main focus of this paper is the cross-coupled voltage controlled oscillator (VCO) core that operates at 2.2 GHz with a 20% tuning ratio. It features a four band frequency tuning characteristic utilizing a binary-weighted switched capacitor bank and metal-oxide semiconductor (MOS) varactors. Power consumption of the VCO core is 20 mW with a tail current of 5 mA and a signal swing equal to 588 mV. Simulated phase noise is -65 dBc/Hz at 100 kHz offset.**

***Index Terms*—Analog integrated circuit, CMOS, digital-controlled oscillators, voltage controlled oscillator, transmitter, RFID tags.**

I. Introduction

RFID is increasingly demanding cheap and robust solutions for its implementation. A 0.5-μm gate-array using a new technology with flexible 20-μm silicon substrates [1] is investigated for its low cost, speed of production, ease of integration and sustainability under mechanical stress.

Active RFID tags consist of an analog front-end and a digital state machine. The digital part can be easily implemented on the sea-of-gates structure, which is intended for a quick implementation of such digital circuits. The radio frequency (RF) front-end; however, presents more of a challenge.

VCOs in CMOS technology using a digital process have been reported in [2], [3], [4]. In this paper, the implementation of two LC VCOs and two CMOS ring oscillators on a sea-of-gates CMOS chip (shown in Fig. 1) using a fully digital process are reported, with focus on the realization of the cross-coupled LC VCO operating at 2.2 GHz.

Section II presents the integrated spiral inductor which has a low quality factor (Q) that accounts for the opted design strategies. Design of the VCOs is detailed in section III. Section IV summarizes the measurement results of the 2.2 GHz LC VCO. In section V, some layout implementation notes are given. This is followed by a conclusion.

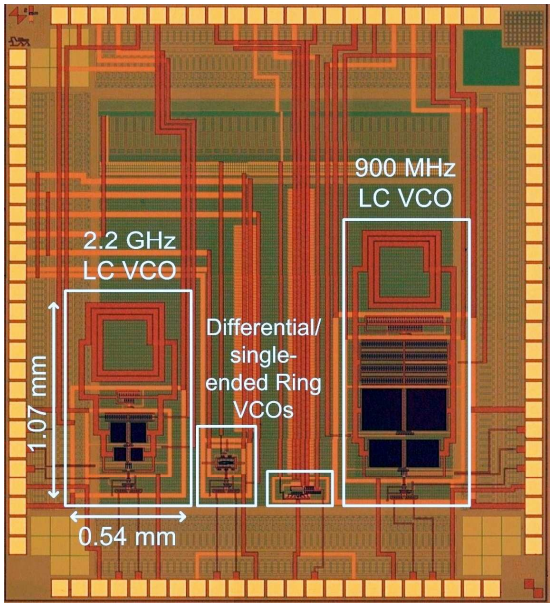

Fig. 1. Die photograph of the fabricated transmitters.

II. Integrated Spiral Inductor

On this technology, the spiral inductors show a low quality factor due to the silicon substrate which increases the losses due to substrate conduction [5]. In addition, the short distance between substrate ground and the top metal layer (900 nm) accounts for a high oxide capacitance value. The following guidelines are followed to optimize the design of the spiral inductor:

- Maximize metal width to reduce series resistance; however, this increases parasitic capacitance to the substrate.
- Use top metal layer since it usually has the smallest resistivity. In addition, this will reduce the parasitic oxide capacitance $(C_{ox} = \frac{\varepsilon_0 \varepsilon_r}{t_{ox}})$ to the substrate since it has a larger distance to substrate ground t_{ox}.
- Minimize metal spacing to increase mutual inductance and occupy less area.
- Maximize inductor opening to limit the effect of eddy currents.

The integrated spiral inductor used in this work has an outer diameter of 434.4 μm and 2.5 turns, with the width and spacing equal to 28.8 μm and 4.8 μm respectively. It is modeled using an electromagnetic (EM) field simulator and verified by fabrication and s-parameter measurements. The measured Q-factor ranges between 3.5 and 3.7 in the used frequency range with an inductance of 4.5 nH at 2.2 GHz. Series resistance and the highly conductive silicon substrate account for the unavoidable low Q-value.

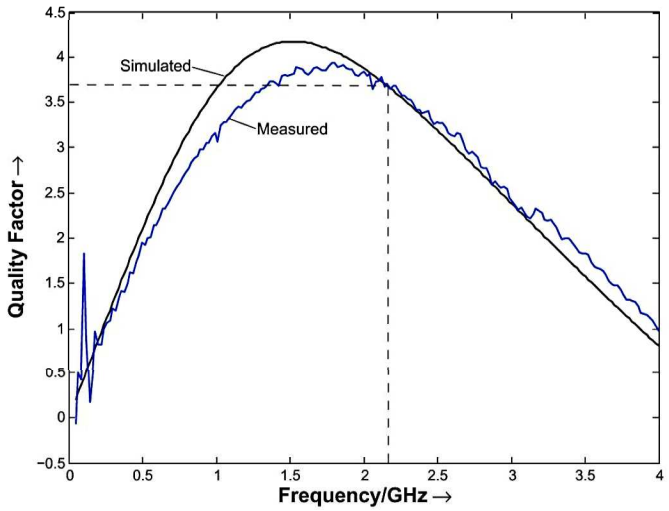

Fig. 2. Measured and simulated inductor quality factor.

Fig. 2 shows the measured and simulated Q-factor for the used inductor. The measured Q-factor is obtained from s-parameter measurements by transforming them into z-parameters on which the definition of the Q-factor is applied.

$$Q = \frac{\omega L}{R} = \frac{Im\{Z_{11}\}}{Re\{Z_{11}\}} \approx \frac{Im\{Z_{22}\}}{Re\{Z_{22}\}} \quad (1)$$

ωL is the inductor impedance and R is the parasitic series resistance. The inductor is a passive device and can be approximated to be symmetrical and reciprocal; therefore, either Z_{11} or Z_{22} can be used in equation 1.

The lumped element model in Fig. 3 is used for circuit simulations [5]. The values for L_s, R_s, C_{ox1}, C_{ox2}, C_{sub1}, C_{sub2}, R_{sub1} and R_{sub2} are obtained by fitting their respective values with the simulation data from the EM field simulator. L_s is the inductance, R_s is the series resistance and elements with the subscripts *ox* and *sub* represent oxide and substrate losses respectively.

III. Design

A. Cross-coupled VCO topology

The VCO core is based on a complementary differential cross-coupled topology with a 5 V power supply and a tunable 5 mA tail current. Implementation is on a two-metal, Manhattan-design, 0.5-μm prefabricated CMOS gate-array structure in bulk silicon. Only the two masks required for structuring the metal interconnects are needed, while the remaining layers are invariable.

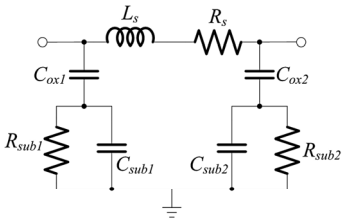

Fig. 3. Lumped element model of a spiral inductor on silicon.

Cross-coupled VCOs operate on the principle of LC resonance. The basic structure of the cross-coupled VCO consists of an LC resonant circuit, negative transconductance components using both NMOS ($M_{n\{1,2\}}$) and PMOS ($M_{p\{1,2\}}$) transistors, a current generation branch ($M_{n\{4,5\}}$), and a current mirroring transistor (M_{n3}). The negative transconductance components are responsible for the compensation of the resonant tank losses by having an equivalent negative resistance ($R = \frac{-2}{g_m}$; g_m is the transconductance of the transistors) designed to cancel out the LC tank parasitic resistance.

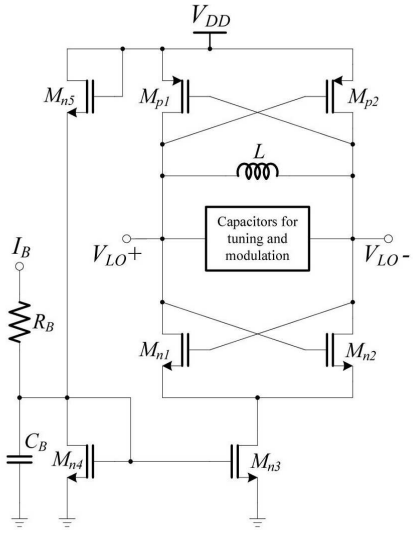

Fig. 4. Schematic of the LC VCO core.

B. Capacitors for frequency tuning and modulation

As shown in Fig. 5 the resonator features a 2-bit binary weighted switched capacitor array for discrete frequency tuning [6], large varactors for analog tuning within each frequency band, small varactors for frequency-shift keying (FSK) modulation and a fixed capacitor.

To maximize the frequency tuning range, both continuous frequency tune and discrete frequency tune are employed. By toggling the MOS switches (M_{n12-17}), the capacitance can be varied from C to 4*C. This results in four frequency bands, thereby increasing the tuning range while lowering the tuning sensitivity (K_{VCO}), which leads to improved phase noise performance [6] and a finer control of the tuned frequency.

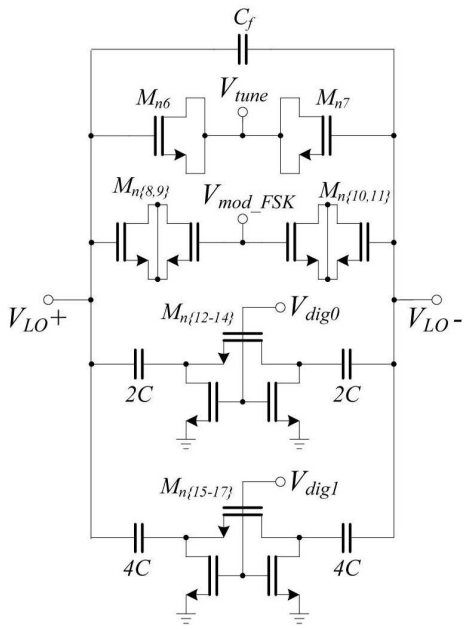

Fig. 5. Details of the capacitor bank in the cross-coupled LC VCO.

The MOS switches are designed using three transistors; two are placed to assure that the switch transistor drain and source are grounded when switched on, each consists of one finger. The third (top) transistor is scaled in proportion to its corresponding capacitors. As it is clear from Figs. 4 and 5, symmetry is ensured at every node to avoid jitter. The designed inter-digital finger capacitors are of a very high quality factor and show near ideal behavior in the relevant frequency range.

MOS varactors are realized by connecting the bulk of an NMOS transistor to the ground with the source and drain tied together. This results in a higher quality factor and a wider tuning range than their conventional p-n junction counterparts [4]. Capacitance ranging from 135 fF to 723 fF is achieved by using fifty fingers of NMOS transistors with a channel width and length of 7.6 μm and 0.5 μm. Furthermore, a dedicated small varactor consists of two back-to-back MOS transistors of one finger each, consequently halving their effective capacitance to 3.5 fF resulting in a smaller frequency shift of roughly 50 kHz used for direct FSK modulation.

C. Buffer, Amplitude Shift Keying (ASK) Modulation Stage and Output Driver

The output stage is designed to drive a 50 Ω load, which is also the termination of most measurement equipment. A buffer with small input transistors is placed to isolate the local oscillator (LO) signal and avoid frequency pulling. Optional ASK modulation is possible by varying the current through a current mode logic (CML) amplifier as shown in Fig. 6. This is followed by a source follower with large transistors to provide enough current and a peak-to-peak voltage of at least 0.5 V for the 50 Ω load.

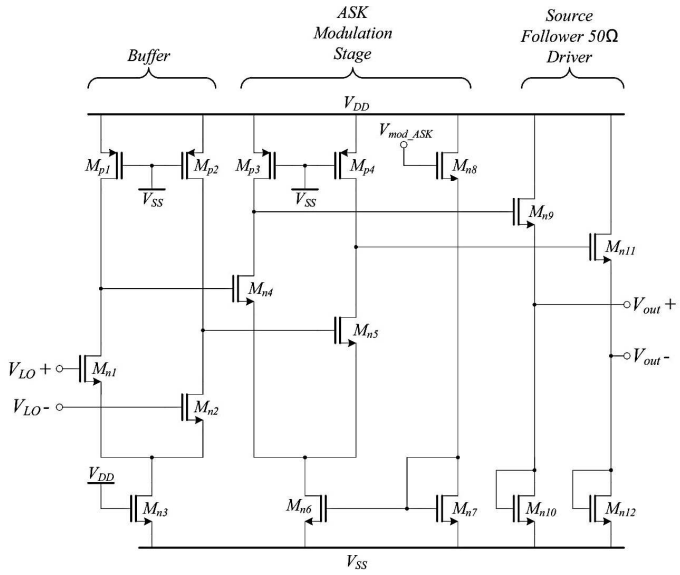

Fig. 6. Output amplifier and ASK modulation stage.

IV. Measurement Results

As a first prototype on this new technology, performance was not targeted. The aim was to compare the different VCOs and to choose a suitable structure and frequency of operation for further development. Additionally, it was required to verify that this technology is suitable for the design of RF circuits since this gate-array structure is usually used for digital circuit designs.

Fig. 7 shows the measured tuning characteristic of the 2.2 GHz LC VCO. Frequency of operation can be varied from 1.775 GHz to 2.189 GHz; a tuning ratio equal to 20% and a K_{VCO} of about 50 MHz/V to 100 MHz/V within each frequency band. A larger tuning ratio of 41% is achieved with the same LC VCO designed for 900 MHz. The measured frequency spectrum is shown in Fig. 8. Simulated phase noise is -65 dBc/Hz at an offset of 100 kHz. Power consumption of the transmitter is around 100 mW with a peak-to-peak voltage of 590 mV when driving the 50 Ω termination of the measurement equipment. This is clear from the real-time scope plot in Fig. 9. The VCO core requires about 20 mW while the remaining power is consumed by the current-mode logic (CML) buffer and driver circuit. Die to die variations were minimal and thus neglected.

These measurements were done on a chip that is manufactured in conventional bulk silicon substrates. The behavior of the RF circuits is expected to improve when tested on ultra-thin silicon [1] due to reduced substrate capacitance and losses. These enhancements are expected to reduce power consumption and increase the frequency of operation.

V. Layout Considerations

The chip layout is optimized for testing by making output pads of the same type on the same side of the chip. This speeds up testing on a wafer prober since the probes can be relocated quickly between transmitters.

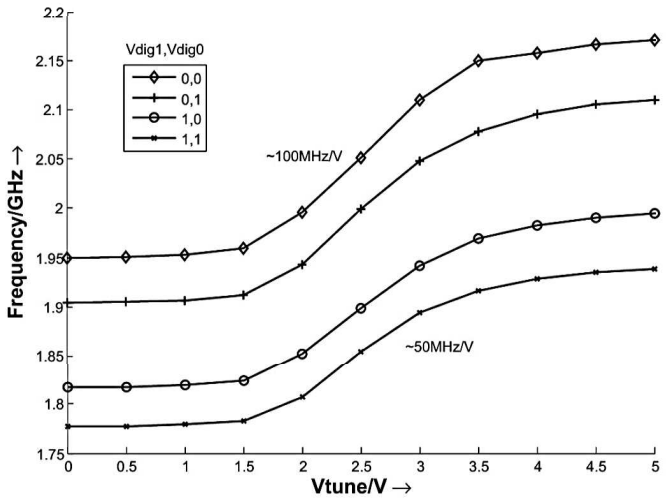

Fig. 7. Measured tuning characteristics of the 2.2 GHz LC VCO.

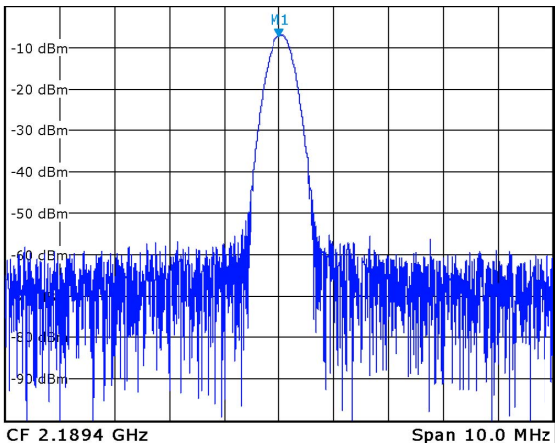

Fig. 8. Frequency spectrum of the 2.2 GHz LC VCO operating at 2.19 GHz. (Frequency response shape is limited by the radio-bandwidth filter of the spectrum analyzer.)

The layout of the differential transmitters is designed to be symmetrical to avoid signal skewing. For the purpose of matching in the cross-coupled transistors, the two transistors are split into fingers which are interleaved together to reduce mismatch offsets. In addition, noise filters are placed on the tuning inputs and the supply rail for a stable power supply.

VI. Conclusion

This paper presents a 2.2 GHz cross-coupled VCO fabricated on a digital sea-of-gates structure. Moreover it discusses the potential of using it in a new technology for the implementation of RFID tags. The design is meant to test the performance of the new technology in dealing with analog and RF transmitter circuits while examining its capabilities in terms of operating frequency, power consumption and frequency tuning range. Measurements on the first prototype show a highest frequency of 2.2 GHz, a wide tuning range of

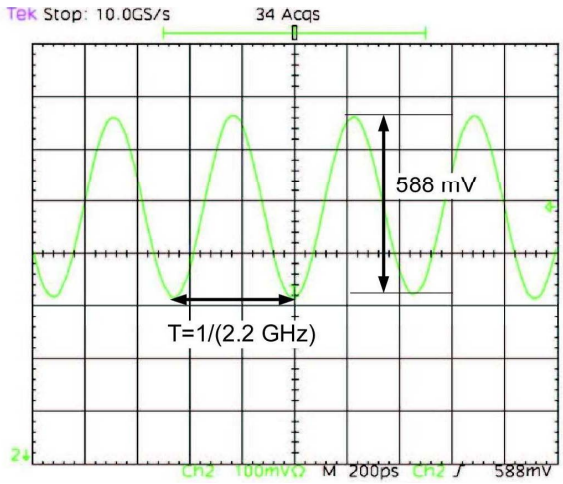

Fig. 9. Real-time scope measurement of the 2.2 GHz cross-coupled VCO at 10 Gs/s.

20% and 40%, power consumption of 20 mW, and an output signal amplitude of 590 mV.

VII. Acknowledgements

The authors would like to thank Dipl.-Ing. Alexander Braekle for his help in device characterization, modeling and measurements.

References

[1] H. Richter, H. Rempp, M.-U. Hassan, C. Harendt, N. Wacker, M. Zimmermann, and J. Burghartz, "Technology and design aspects of ultra-thin silicon chips for bendable electronics," in *IC Design and Technology (ICICDT). IEEE International Conference on*, May 2009, pp. 149 –154.

[2] A. Dec, H. Akima, and K. Suyama, "A 5 GHz LC VCO with extended linear-range varactor in purely digital 0.15 μm CMOS process," in *Radio Frequency Integrated Circuits Symposium (RFIC). IEEE*, Jun. 2009, pp. 567 – 570.

[3] T. Melly, A.-S. Porret, C. Enz, and E. Vittoz, "A 1.2 V, 433 MHz, 10 dBm, 38% global efficiency FSK transmitter integrated in a standard digital CMOS process," in *Custom Integrated Circuits Conference (CICC). Proceedings of the IEEE*, May 2000, pp. 179 –182.

[4] Y. Choi, T. Teo, and W. Yeoh, "A 2.4 GHz fully integrated CMOS VCO with direct FM/FSK modulation capability," in *Electron Devices and Solid-State Circuits, IEEE Conference on*, Dec. 2003, pp. 175 – 178.

[5] J. Burghartz, D. Edelstein, M. Soytter, H. Ainspan, and K. Jenkins, "RF circuit design aspects of spiral inductors on silicon," in *Solid-State Circuits Conference. Digest of Technical Papers. IEEE International*, Feb. 1998, pp. 246 –247, 443.

[6] H.-K. Chiou, H.-J. Chen, H.-Y. Liao, S.-G. Lin, and Y.-C. Chang, "Design formula for band-switching capacitor array in wide tuning range low-phase-noise LC-VCO," *Microelectronics Journal*, vol. 39, no. 12, pp. 1687 – 1692, Jul. 2008.