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Design of an RF Transmitter for RFID Tags in a New Technology with Ultra Thin Silicon Substrates

Bachelor Thesis

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Abstract

The development of the Gateforest® technology with new ultra-thin silicon substrates triggered research into its possible applications. RFID implementation, specifically the transmitter implementation, on this technology is investigated in this document. To start with, the measurement and simulation of circuit elements (passive and active) at high frequencies is done in order to verify that the chip could operate at radio frequencies. The document then discusses the basic structures that are involved in the design of the transmitter test-structures, followed by the theory of operation of voltage controlled oscillators. The implementation of the circuits is done to explore the possibility of creating an RFID tag using a new technology. For this, 4 transmitter circuits are designed, two ring oscillators and two cross-coupled oscillators, such that they cover 3 different operating frequencies (433 MHz ISM band, 869 MHz SRD band and 2.45 GHz ISM band). They are also designed in both differential and single-ended form to cover a good set of different parameters for testing. In circuit design, high complexity of the structures is avoided because this is only a first prototype and special care was taken in order to provide a wide tuning range ($\geq 40\%$). This is important in order to assure that the operating frequency could be reachable despite temperature and process variations. The circuit layout is done such that it fitted on one chip provided by *IMS-CHIPS*. The pad connections are done so that testing of the chip is facilitated as much as possible.

Acknowledgments

Throughout the work in this bachelor project, I have learned to appreciate the help and support offered by many people who deserve special mention at the beginning of this thesis.

To start with, I am grateful to the German University in Cairo (GUC) for providing the opportunity of studying in Stuttgart. My gratitude also goes to the DAAD for funding and the University of Stuttgart for maintaining a partnership with the GUC, and offering me the bachelor topic which is the subject of this thesis.

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Alex: For the help with measurements and simulations, and for showing me how to create tidy plots for my thesis and presentations.

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My friends were unbelievable in making me feel at home, and always being there for me, and for generally always being so much fun to be around! I extend my heartfelt thanks to: Allouba, Eaka, Eslam, Esso, Ghada, Maggie, Mahi, Mahy, Mariam, Mostafa, Sarah, Shalaby and Tcheva.

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Nomenclature

μ_n Electron mobility in a transistor, page 6

τ RC Time constant, page 56

A_v Voltage Gain, page 22

AC Alternating Current, page 6

C_{ox} Oxide capacitance of a transistor, page 6

DC Direct Current, page 6

f_c Cutoff frequency specifying the bandwidth, page 25

g_m Transconductance of a transistor., page 6

HF High Frequency, page 6

I_{DS} Drain to source DC current of a transistor, page 6

K_{VCO} Tuning sensitivity of an oscillator, page 47

Q Quality Factor, page 11

$R_{\square}$ Square resistance, page 14

$RFIC$ Radio Frequency Integrated Circuit, page 11

V_T Thermal voltage of a transistor, page 6

V_{DS} Drain to source DC voltage of a transistor, page 6

V_{GD} Gate to drain DC voltage of a transistor, page 6

V_{GS} Gate to source DC voltage of a transistor, page 6

V_{id} Differential input voltage, page 23

$V_{in,CM}$ Common-mode voltage level, page 22

V_{pp} Peak-to-peak voltage of an AC signal, page 76

V_{th} Threshold voltage, page 51

ASK Amplitude Shift Keying, page 61

BW Bandwidth, page 28

CE Circuit Envelope simulation profile in Agilent Advanced Design Systems, page 74

CML Current Mode Logic, page 22

EM Electromagnetic, page 1

FSK Frequency Shift Keying, page 61

G Ground, or V_{SS}, used as an abbreviation in the pad labels, page 117

HB Harmonic Balance simulation profile in Agilent Advanced Design Systems, page 74

ID Identification, page 1

ISM International scientific and medical bands, page 47

L Transistor channel length, page 6

LC The L stands for inductance, and the C for capacitance, LC denotes a (sub)circuit which contains these components, page 31

LF Low Frequency, page 25

LO Local oscillator, page 50

ov Overlap of different frequency bands, page 54

P Power, or V_{DD}, used as an abbreviation in the pad labels, page 117

PLL Phase Locked Loop, page 120

RC Resistor and capacitor, page 17

RFID Radio Frequency Identification, page 1

S Signal,input or output, used as an abbreviation in the pad labels, page 117

Si   Silicon, page 2

TR   Frequency tuning range of an oscillator, page 55

VNA   Vector Network Analyzer, page 3

VTC   Voltage Transfer Characteristics, page 21

W   Transistor channel width, page 6

Chapter 1

Introduction

1.1 Background

Identification(ID) systems find applications in retail, surveillance, tracking, toll collection, medicine, key-less entry and many other authentication-requiring services [3]. Formerly, bar codes were the industry standard in providing such identification for an automated system, this method however had many disadvantages. Bar codes could only store a very small amount of information, they require line-of-sight operation and although they are easily produced by printing, they are not robust and are not suitable for all weather conditions [3].

1.1.1 RFID Systems

The new solution replacing bar codes is Radio Frequency Identification (RFID) which overcomes the mentioned disadvantages, and takes wireless data transfer to a new level. RFIDs operate on the same principle as most of today's wireless communication systems; they are composed of a transmitter and a receiver with data transferred between them in the form of electromagnetic (EM) waves [3].

A more abstract view of an RFID system can be done by assuming an RFID tag and a reader. The RFID tag is composed of a transmitter and a receiver which *reads* an incoming signal (from the reader) and transmits a reply accordingly. This reply can contain a security code, a price or any kind of information, thus performing the job of an electronic ID system.

The advantages brought forward by this new technology is that it provides a wireless method of data transfer which is independent of weather conditions, does not require line-of-sight, has a long range, can store a lot of information and is overall more robust and quicker than bar codes. The challenges brought forward by RFID systems is to be able to design a tag as small as possible, flexible so it does not break easily, has a long range, is power efficient and can be cheaply

mass produced as well.

1.1.2   The Gateforest® Technology

The technology used in this work is provided by the vendor IMS-CHIPS, it is a preprocessed chip consisting of an array of gates in a sea-of-gates structure making up most of the chip area. This is shown in fig. 1.1 as the digital section, there is also a small analog section north of the chip. The digital-core transistors are smaller ($0.5\mu m$) and faster than the analog ones, making them suitable for use at the RF frequencies required in the designs. It was nonetheless crucial to measure their RF parameters so that they are verified to the model and can be used in simulations, this is done in chapter 2.

The analog section consists of resistors as well as capacitors along with the larger transistors organized in cell structures each with a specific number of each component.
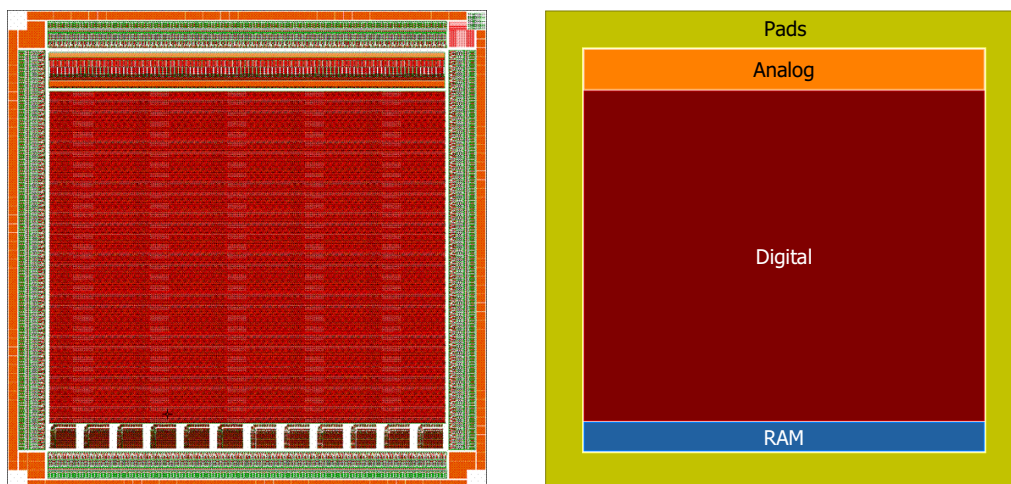
Figure 1.1: Layout of a Gateforest® master core [1].

Gateforest® technology is now being fabricated on the new ultra-thin Silicon (Si) substrates ($20\mu m$). This makes it smaller in size and more flexible as well which is of great advantage when applied to the production of RFID tags. The fabrication process is also done cheaply in a new process [1].

1.2   Motivation

Since RFID is increasing in popularity, and becoming more and more widely used: cheap and practical solutions for its production must be sought out. The
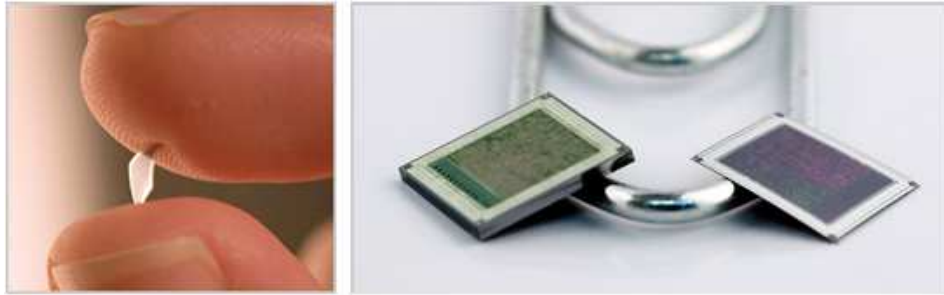
Figure 1.2: Ultra-thin silicon.

new technology mentioned provides many advantages in that regard. Since it has a thin substrate, it can be easily embedded in such products as ID cards and price tags. The speed of the transistors is adequate to operate RFID at any of the allowed bands. It is also cheap since the chips are produced with the thin-film Si technology [4]

1.3 Simulation Software and Measurement Equipment

Many computer-aided design tools are used in this project, they are listed below.

1. Agilent™ Advanced Design System (ADS): This is used for schematics and schematic-level simulations.

2. Cadence™ Virtuoso: Used for circuit layout.

3. ADS Momentum: Add-on for ADS which is used for EM simulation of inductor and capacitor test structures before measurements.

4. Cascade™ Microtech Wincal 3.1.0.31 VNA Calibration Software.

5. Cascade™ Microtech Prober Control Software (PCS) Utility.

Hardware Measurement equipment, listed below, are also used in the measurements.

1. Cascade™ Microtech Microchamber Probing Station.

2. Hewlett Packard™ 8510B Vector Network Analyzer (VNA).

3. Hewlett Packard™ 4155B Semiconductor Parameter Analyzer.

1.4   Thesis Organization

This document is focused on the design of a transmitter fitting to the specifications of the mentioned technology. The text takes the steps of the design in the order in which they were investigated. Starting with the modeling and measurements of the test-structures, then moving on to the necessary theory of oscillators followed by how it was applied on the designed circuits. Furthermore, a chapter including simulation results, emphasize the important results that characterize the designed transmitters. Layout considerations are then discussed and finally the thesis is then briefly summed up in the last chapter.

Chapter 2

Integrated Circuit Components

This chapter presents the first step performed before the actual circuit design. It is imperative to test the various components of this new technology so as to verify their properties, create simulation models and verify that they can operate at the required frequencies.

Measurements are performed on a Gateforest® testchip with various passive and active structures of different sizes. A photograph of this chip is shown in fig. 2.1
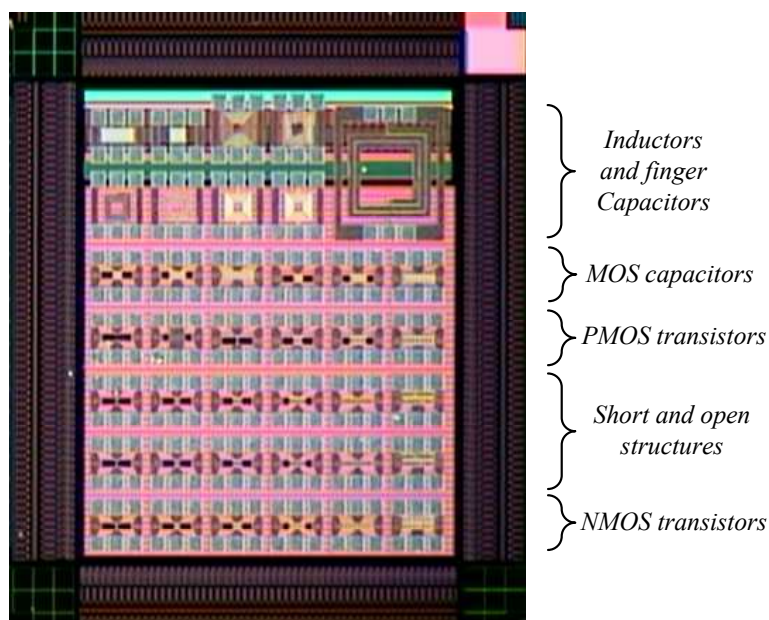
Figure 2.1: Micrograph of the measurement testchip.

2.1   Transistors

The transistors used in this work are part of the digital core in a Gateforest®
gate-array chip, and since it is a new technology, some essential tests and simu-
lations were required to be run on the transistor preparing it for circuit design.
It is essential to verify the transistor model used, and since the chip was mainly
used for digital circuits before, it is of especially high importance to validate the
high-frequency (HF) parameters in the transistor model.

2.1.1   DC and AC Characteristics

Typical direct-current (DC) characteristics are displayed through a graph of
drain-source current (I_{DS}) vs. drain-source voltage (V_{DS}). This characteristic,
which is shown in fig. 2.2, is simulated in the operating region of the transistor
(0V to 6V for NMOS and 0V to -6V for PMOS), and is plotted for different
values of gate-source voltages (V_{GS}).

For some applications, as it is the case in this work, the transistor may be
used as a resistor. In this case the gate and drain are connected, converting it to
a two-terminal device and forcing the gate-drain voltage (V_{GD}) to be zero. The
condition for transistor operating in saturation region is

$$V_{DS} \geq V_{GS} - V_T,$$

and we have

$$V_{GD} = 0,$$

therefore the transistor will always be in pinch-off mode when connected in this
configuration. This connection is utilized in voltage-to-current conversion in the
current generation branch of a current source. Fig. 2.3 shows the resistance of
the p-channel and n-channel transistors varying with drain-source voltage. It
is shown to be quite constant in the operating voltage range, although it is a
non-linear function of voltage.

$$R_{eq} = \frac{V}{\mu_n C_{ox} \frac{W}{2L} (V - V_T)^2} \tag{2.1}$$

Resistance is plotted for different channel widths, this has the same effect as
connecting transistors in parallel; resistance is halved when width is doubled.

A very important alternating current (AC) parameter of a transistor is the
transconductance (g_m). G_m is simulated for different values of V_{GS} and plotted
against V_{DS}. It is significant because it gives an indication of the small-signal
gain, and is generally required for the sake of completeness of the transistor
analysis.
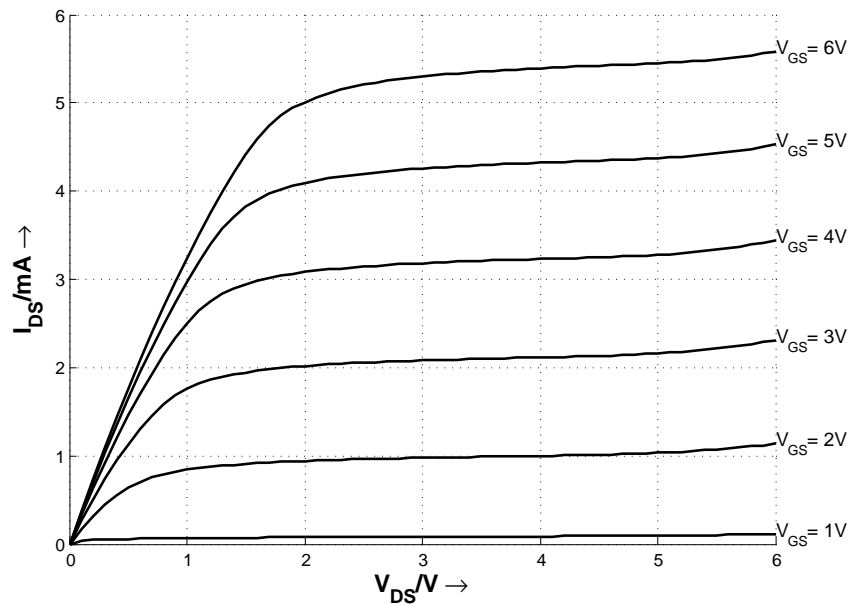
(a) NMOS
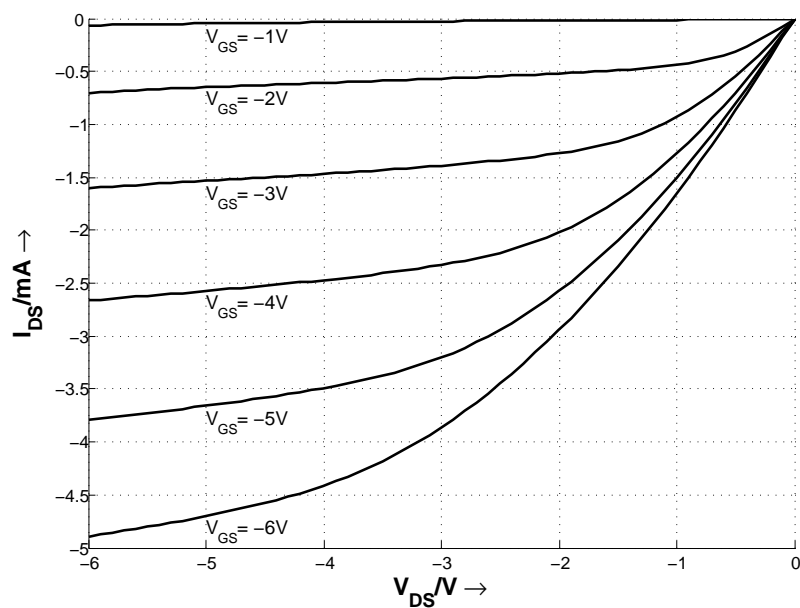
(b) PMOS

Figure 2.2: Simulated transistors I-V characteristics: I_{DS} versus V_{DS} for different values of V_{GS}.
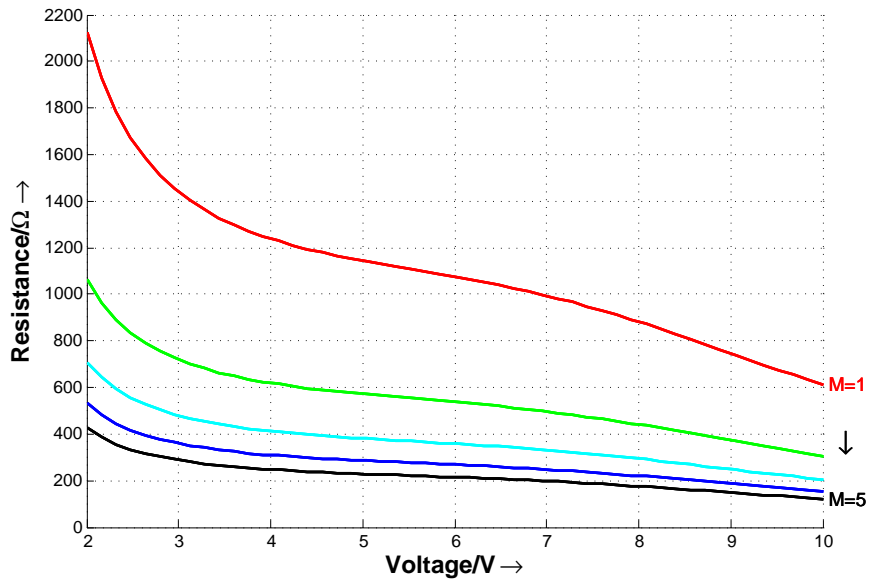
(a) NMOS
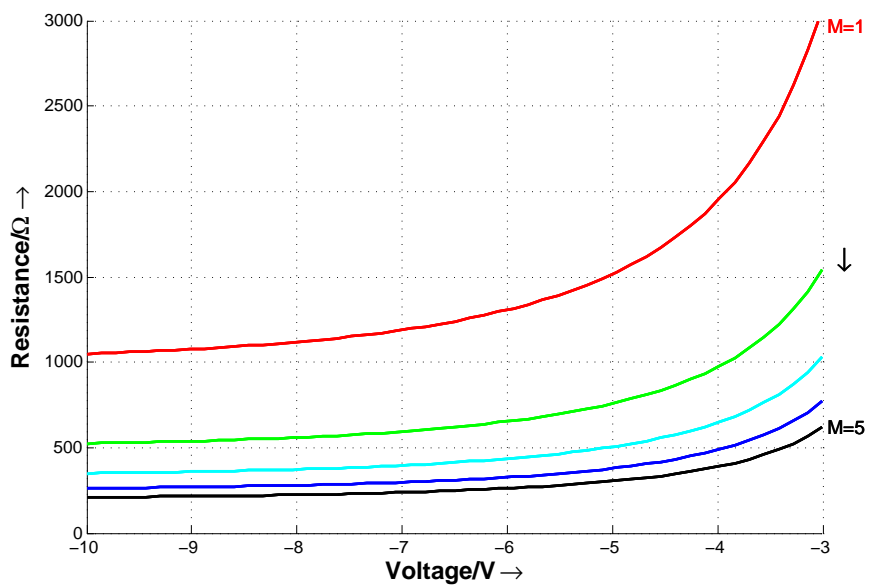
(b) PMOS

Figure 2.3: Simulated resistance of the transistors versus V_{DS} for different channel widths, M shows how many transistors are connected in parallel.

(a) NMOS

(b) PMOS
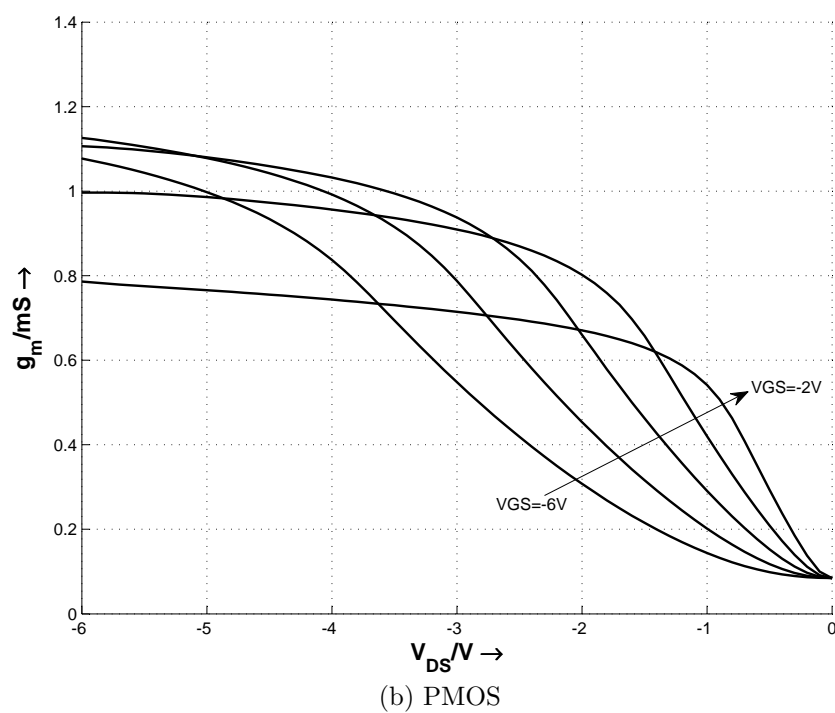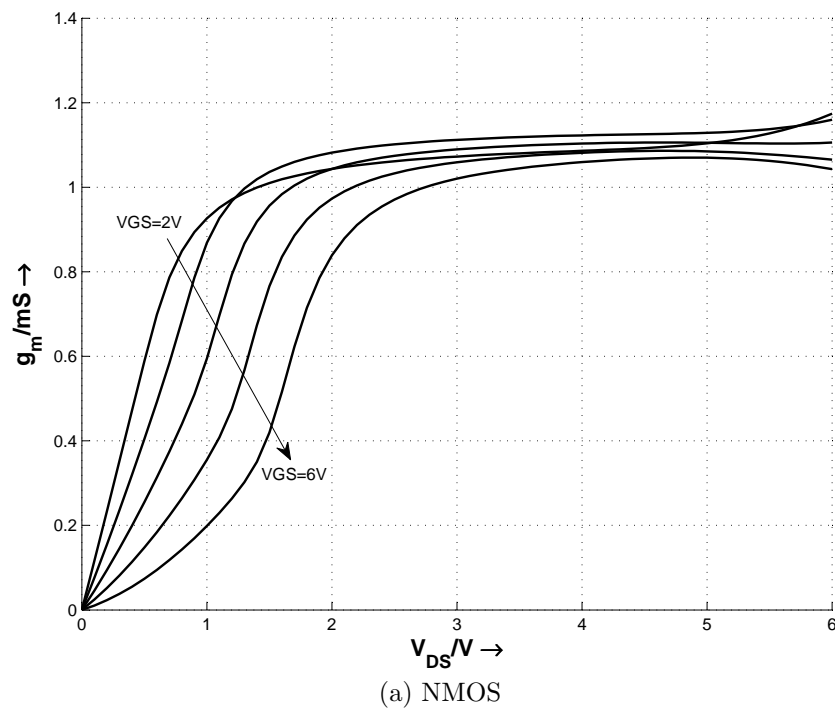
Figure 2.4: Simulated transconductance of the transistors versus V_{DS} for different values of V_{GS}.

2.1.2   HF Measurements and Simulations

Transistors used in this work were only previously used for digital circuits in which the frequency of operation is related to the data rate, which of course is not an RF frequency as it is required to be in the transmitter circuits.

To get an indication of the speed of the transistor it is enough to measure the transit frequency of the transistor. Transit frequency is the frequency at which the transistor's current gain drops to unity while the source and drain terminals are held at signal ground [5]. The current gain is the ratio of the drain current to the gate current; while the drain current is frequency independant, the gate current increases proportionally with frequency which is why the slope of a typical current gain curve is -20 dB/decade.

Transit frequency is important to measure because it shows how fast a signal change at the gate of the transistor, which is usually the input, reflects on the output. For this HF parameter, several measurements are made on the test chip to verify the transistor model. S-parameter measurements are done on the test chip transistors, measurements are made for three different chips from different ends of the wafer to investigate any position effects. All the NMOS transistor structures where biased at voltages of $V_{DS} = 3.5V$ and $V_{GS} = 3.5V$ as well, while PMOS is biased with $V_{DS} = 3.5$ and $V_{GS} = -2.0V$. The methodology in verifying the transit frequency is as follows [6]:

1. S-parameter measurements were made on the VNA for different transistor sizes and positions.

2. S-parameter measurements were conducted on the open structures corresponding to the measured transistors.

3. Data is exported to the simulation tool for manipulation; the Y-parameters were calculated.

4. To find the transistors S-parameters excluding the pads: The Y-parameters of the open structures where subtracted from the complete transistor (with pads) Y-Parameters, resulting in what is therefore the Y-parameters of the transistors themselves, with the pads effects de-embedded. They are then converted back to S-parameters.

5. The transistor model's current gain is simulated and compared with that of the measured values.

Plots of simulated and measured current gains, with and without de-embedding the pads, are shown in figures 2.5 and 2.6 for n-channel and p-channel transistors respectively. It can be seen that the measured and simulated values were close;

the measured values displayed higher transit frequencies than the simulated ones, making the model a pessimistic one, suitable and safe for use in simulations.

In the 2 finger transistors the current gain and transit frequencies were higher than expected after de-embedding, and lower than expected before. This is due to the effect of the pads which is more dominant in the small transistor, it overshadows the transistor's characteristics itself. As can be seen in the 34 finger transistors, the effect of de-embedding is much less and the measured values were closer to the simulated ones. PMOS transistor measurements showed generally better HF behavior than the model.

For the measured plots there is some distortion and unexpected behavior at low frequencies; the reason for this is the inaccuracy of the VNA measurements at low frequencies. Note that data becomes invalid after 4 GHz because measurements are only conducted up to that frequency.

2.2   Inductors

Inductors are important performance-limiting components in radio-frequency integrated circuits (RFIC) . The inductor's quality factor (Q) is the most important parameter associated with an inductor, it is defined as the ratio between the imaginary and real parts of the inductor's impedance.

$$Q = \frac{Im\{Z\}}{Re\{Z\}} \tag{2.2}$$

The inductor's Q is an indication of how lossy the inductor is and it usually determines many aspects of a circuit such as power consumption, area and current.

2.2.1   Spiral Inductors

Spiral inductors are used in RFICs, they are implemented on the uppermost metal layer available on a chip, and the connection of the spiral center is done using a lower metal layer crossing [7] as shown in fig. 2.7. Inductors can also be implemented as *stacked* inductors; by connecting more than one metal layer together hence reducing the resistive losses of the coil. Increase of the Q up to 14% is reported in [8]. Inductors of circular geometry were reported to have a higher Q [7], but in most cases as it is in this work, only Manhattan geometries were allowed.

It is still challenging to implement monolithic inductors in RFICs due to the low resistivity of the Si substrates ($\ll$0.01 Ω-cm [9]). Eddy currents induced in the substrate cause the degradation of the Q factor [8]. Monolithic inductors also
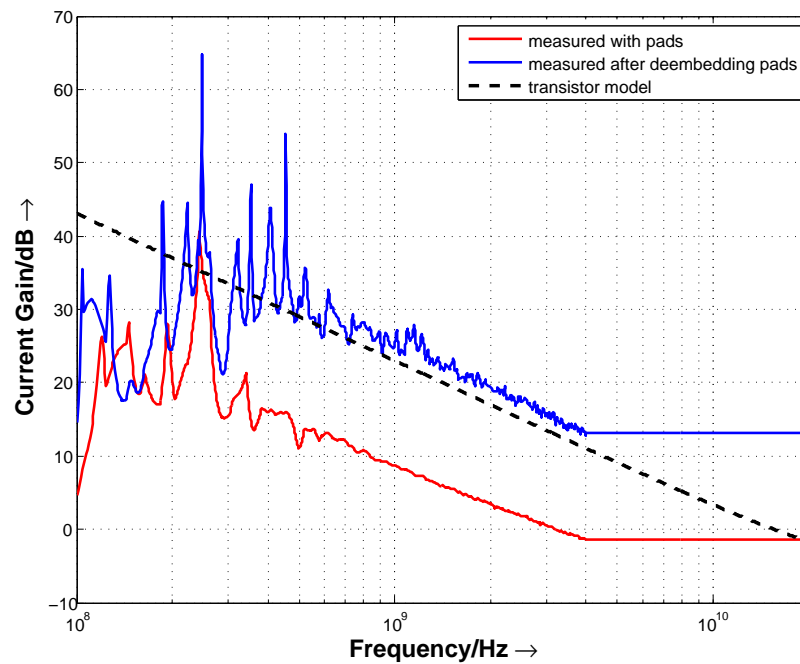
(a) NMOS 2 fingers
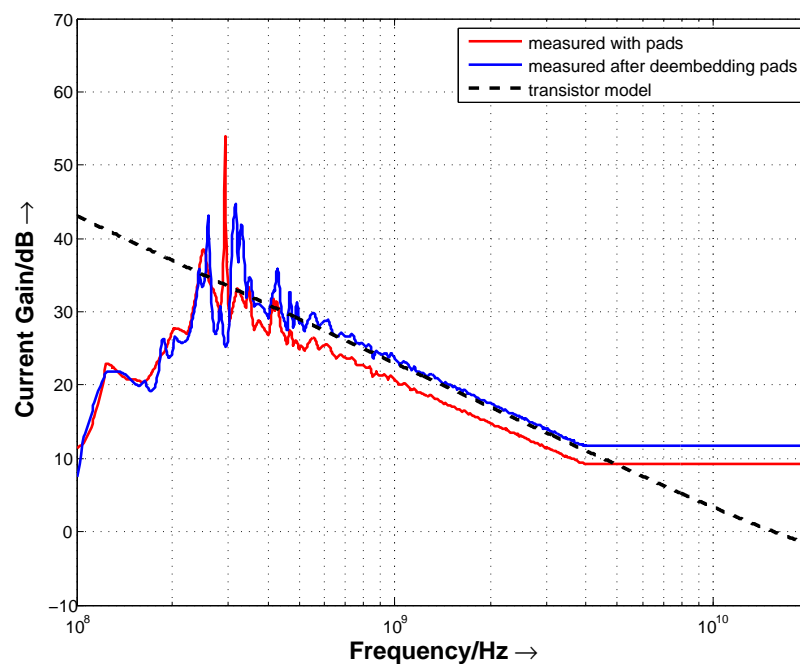
(b) NMOS 34 fingers

Figure 2.5: Simulated and measured (before and after pad de-embedding) current gain curves for different sizes of NMOS transistors.
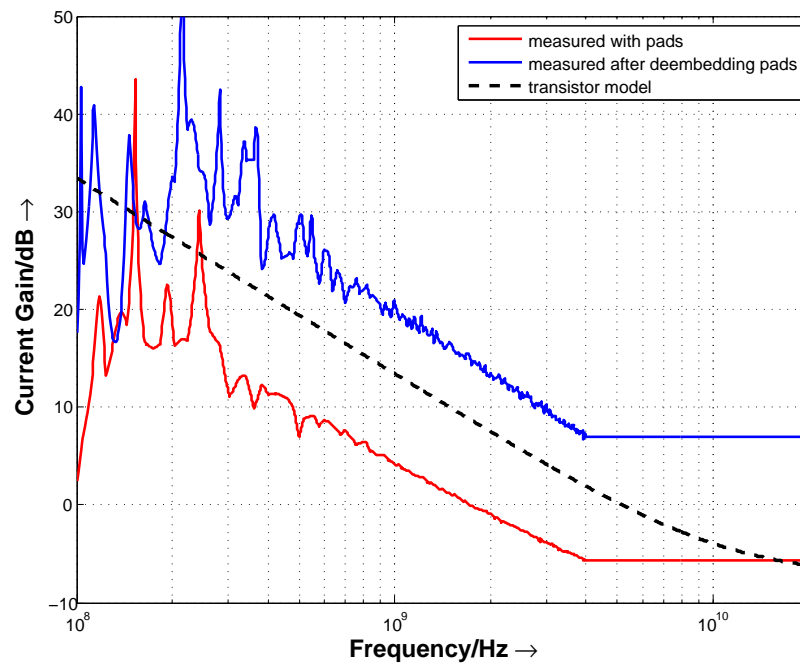
(a) PMOS 2 fingers
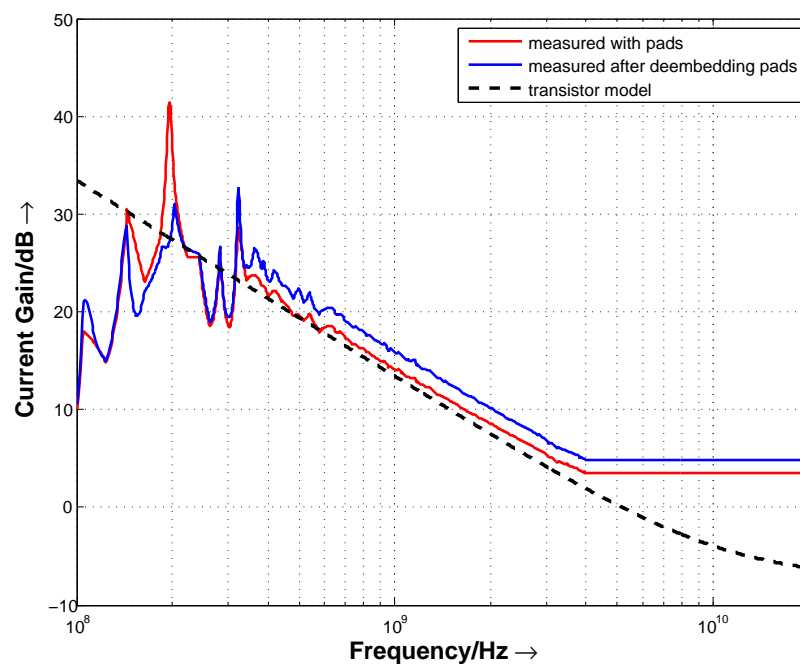
(b) PMOS 34 fingers

Figure 2.6: Simulated and measured (before and after pad de-embedding) current gain curves for different sizes of PMOS transistors.

occupy very large silicon area. In spite of these setbacks, monolithic inductors are still favored to active inductor implementations, since they display lower power consumption and noise, which is usually critical in applications such as oscillators or low noise amplifiers.

a)   b)
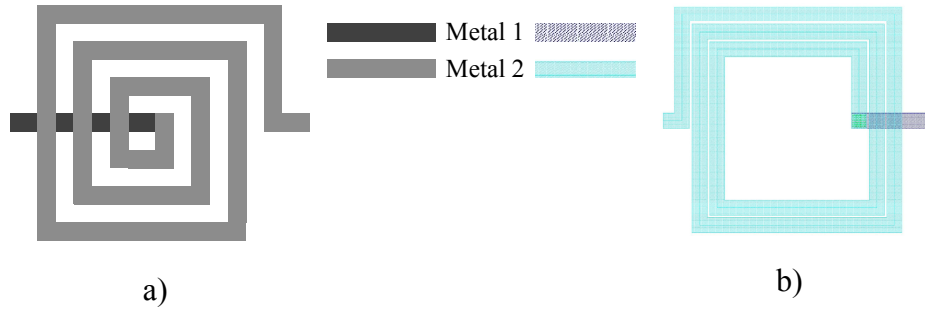
Figure 2.7: a) Layout of a typical spiral inductor. b) Actual layout of the used inductor.
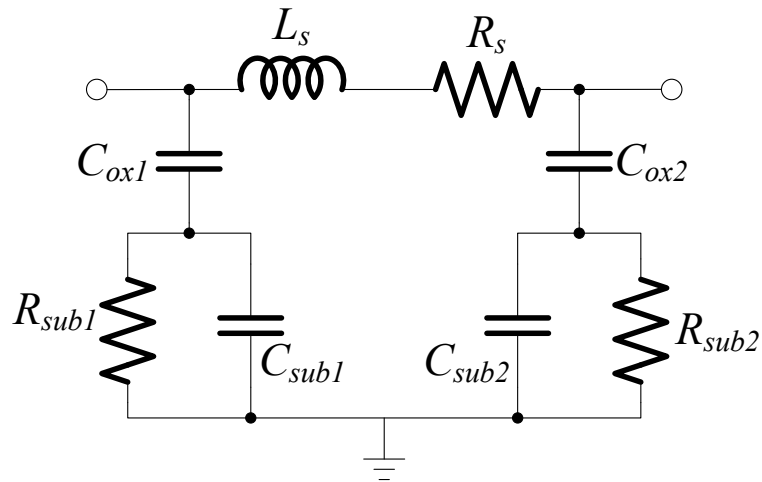
Figure 2.8: Lumped element model of monolithic inductors.

To model the parasitics of monolithic inductors, a lumped-element model is used in simulations. Refer to fig. 2.8. This is a description of the elements:

R_s Series resistance representing the ohmic losses due to the metal wire resistivity, a rough value can be calculated directly using hand calculations by multiplying the square resistance ($R_\square$) by the length and dividing by the

width of the wire used in the inductor.

$$R_s = R_\square * \frac{l}{w} \tag{2.3}$$

C_{ox} Capacitance from the metal to the oxide layer.

C_{sub} Capacitance from the metal to the substrate, here the substrate is considered connected to ground.

R_{sub} Resistance of the Si substrate. As discussed above, eddy currents due to the low resistivity of the substrate degrade the Q of the inductor.

From the measured sample of inductors, the inductor with the highest Q is chosen for use in the designed oscillators. This inductor's properties agreed with the theoretical guidelines for creating a high Q inductor which are summarized in the following points [10]:

- Use of the top metal layer due to the reduced capacitance, since the top metal layer is furthest from the substrate.

- Reduction of the spacing between the metal lines, but an optimum has to be found because at high frequencies the capacitive coupling between the lines increase thus increasing losses.

- Using wide metal to reduce the series resistance. This increases the capacitance as well as the area of the inductor, so an optimum value is required.

- Keep the opening in the middle of the inductor large to reduce eddy currents.

Fig. 2.7 showing the used inductor's layout clarifies how the above criteria are fulfilled. The inductor is simulated with an electromagnetic simulator and measured using the VNA to extract the S-parameters, both were optimized using a simulation tool to fit to the parameters shown in fig. 2.8.

Fig. 2.10 shows a plot of the simulated and measured inductor quality factor. It can be seen that there is a good agreement between the measured and simulated data, after optimization of the inductor's model. The plot shows an optimum Q at about 1.5 GHz. From DC to 1.5 GHz the Q increases on account of increased reactance (which is proportional to frequency $< j\omega L >$). After 1.5 GHz, Q drops once more, this is due to the eddy currents in the highly conductive silicon substrate which dominate at high frequencies.

(a) S11

(b) S12

(c) S21

(d) S22
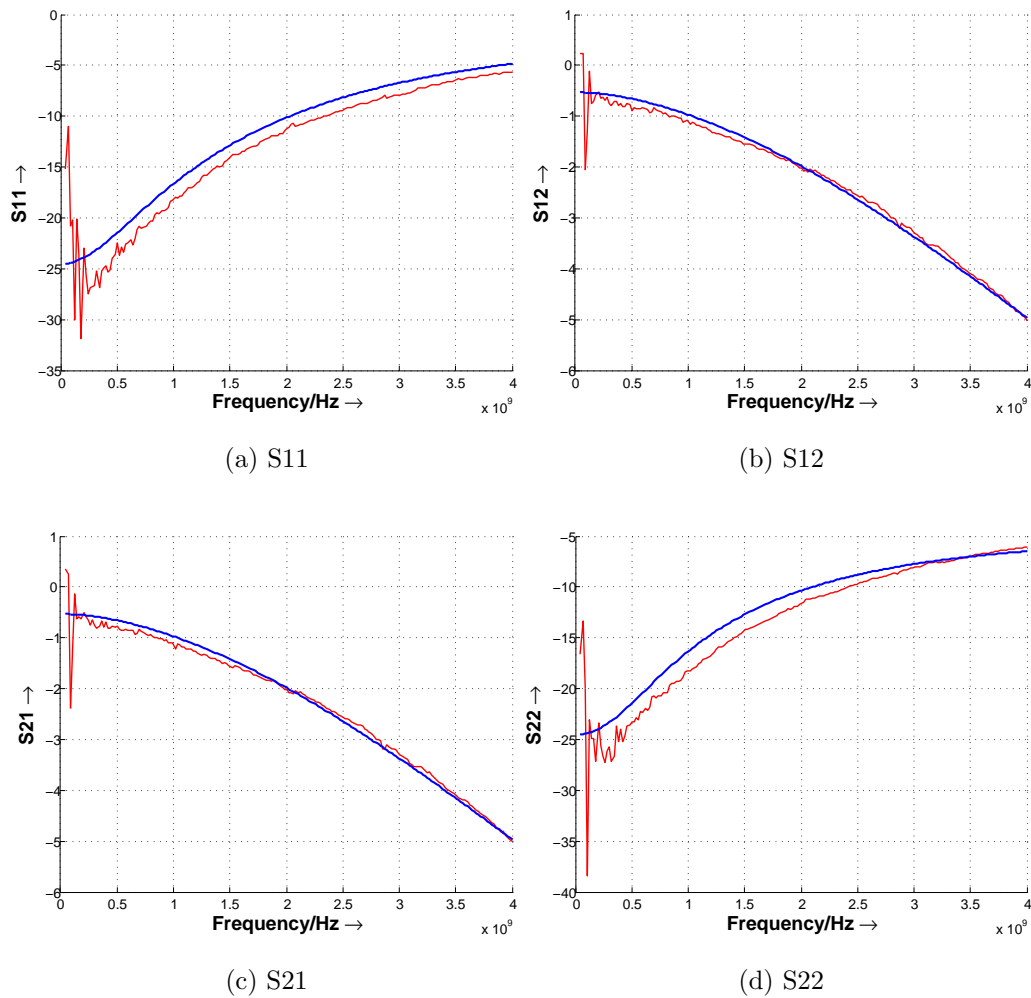
Figure 2.9: S-parameter measurements (red) and simulations (blue) of the used monolithic inductor.
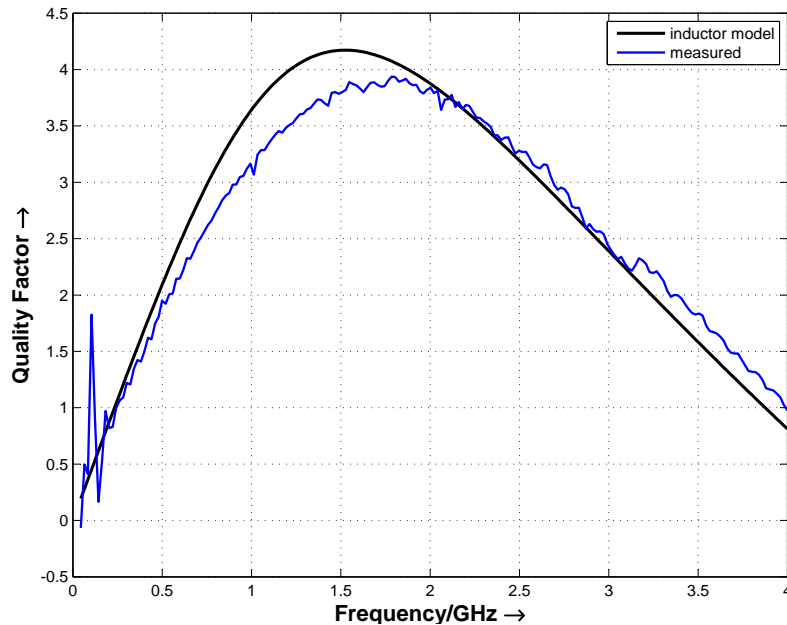
Figure 2.10: Quality factor of the used inductor.

2.3 Capacitors

Capacitors are found in any resonator along with an inductor and is therefore present in any oscillator based on LC structures. For tuning it is sometimes found most convenient to use variable capacitors in place of the fixed ones, although that may also be a cause of poor tuning linearity. Tuned capacitors, or varactors, are discussed in chapter 3. Following is a quick report of the capacitors used in this project.

2.3.1 Poly-poly Capacitors

In the analog section of the chip there were pre-fabricated capacitors with fixed values of about 90 fF for each capacitor shown in fig. 2.11. The fixed capacitors were constructed by using two polysilicon layers; the gate polysilicon and another highly conductive poly-silicon layer which achieves good capacitance. The effective capacitance per unit area is approximately $534pF/mm^2$.

Although the mentioned capacitors are compact and have good Q's, they were unsuitable for use in the oscillators in this circuit. The reason behind this is the fact that the oscillator circuit is required to be symmetrical, and since the analog capacitors had fixed positions at the top of the chip, they were unsuitable for that. These capacitors were however utilized in another way; they were used in constructing the RC noise filters for some of the tuning inputs for the oscillators.

One 90 fF capacitor
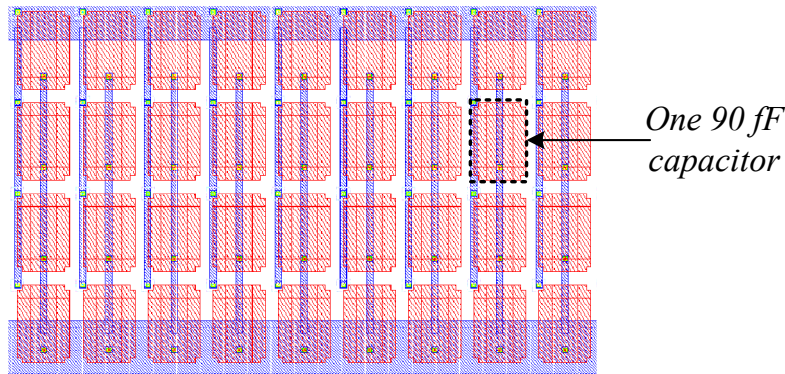
Figure 2.11: Capacitor layout from the analog area, used in RC filters.

2.3.2 Finger Capacitors

Finger capacitors, also called inter-digital capacitors, were implemented among the test structures as they are used in most oscillator structures. They are implemented using two metal layers to maximize capacitance and reduce resistance. As shown in fig. 2.12, the capacitor is arranged in form of fingers with both metal layers on top of one another. The capacitance is directly related to the capacitor layout area and is estimated from the measurment data at about $30pF/mm^2$.
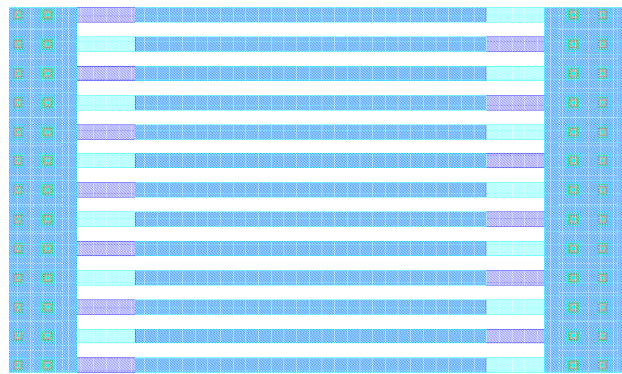
Figure 2.12: Interdigital finger capacitor used in the LC resonator.

The quality factor of the finger capacitors, which is defined the same way as that of the inductors (eqn. 2.2), is found to be very good making it valid to use an ideal capacitor component in simulations.

Chapter 3

Basic Circuits

3.1 Varactors

Varactors, which are also called *vari-cap* diodes, are called so as an abbreviation for variable capacitors. Their operation depend on the variation of voltage across a reverse biased diode structure thereby controlling the depletion capacitance of such a structure.

a)   b)
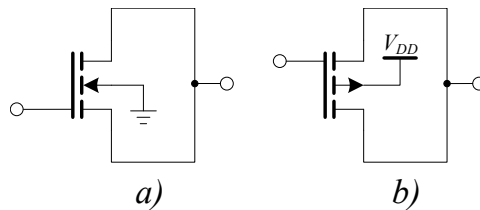
Figure 3.1: Schematics of the a) n-channel and b) p-channel varactors.

Varactors can be fabricated as diodes on the silicon chip by having n-type and p-type diffusions like a normal diode. As an alternative, which is applied in this work, a normal transistor could have its source and drain terminals connected (and sometimes the bulk as well) to form a diode structure as shown in fig. 3.1. It can also be seen from the figure that for this work, connecting the bulk connection along with the source and drain is not possible because all bulk connections are connected together either to V_{DD} or V_{SS}. We can distinguish between three different modes of operation as shown in fig. 3.2. They are summarized below.

- **Accumulation mode:** This occurs when $V_{GS} < 0$ and in this operation mode the voltage on the gate oxide is high enough to allow electrons to move freely. The electrons are *accumulated* on the gate oxide interface therefore the equivelant capacitance is only that of the oxide insulator

where $C_{ox} = \frac{\epsilon S}{t_{ox}}$ (S and t_{ox} are the gate channel area and oxide thickness respectively).

- **Depletion mode:** This area of operation is the one utilized for capacitor tuning mainly, it occurs when $0 < V_{GS} < V_{th}$. When a voltage from this range is applied the electrons move away from the oxide interface, or are *depleted* in this area, resulting in an additional capacitance effectively being in series with the oxide capacitance thereby reducing the value for total capacitance. Note that between the electrons and gate oxide there still is no conductive channel layer and this is why this depletion capacitance is observed.

- **Inversion mode:** When we further increase the voltage to $V_{GS} > V_{th}$ the channel now forms at the gate oxide and effectively cancelling the depletion capacitance. This happens because what used to be a kind of dielectric layer for the capacitor is now a conductive area, the total capacitance therefore goes back to C_{ox} as in the accumulation region.
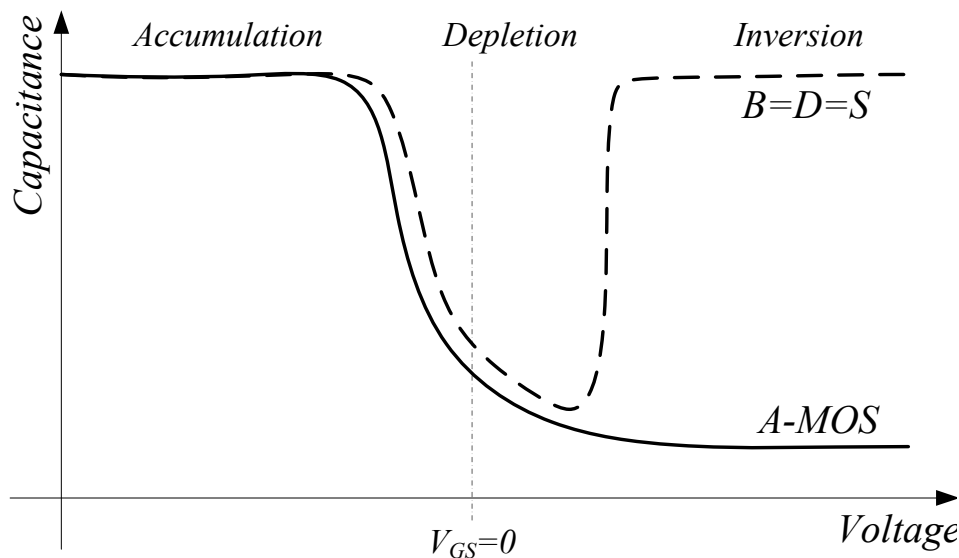
Figure 3.2: Capacitance of a varactor versus voltage.

Varactors used in this work follow the curve marked with A-MOS, they never enter inversion mode because their bulks are connected to ground [11], this has the advantage of a wider tuning range as it is apparent from the plot. A mirror image of this curve could also be obtained by connecting the bulk connection to V_{DD} instead of ground.

3.2   Amplifiers

This section presents some basic sub-circuits which were used mainly in the output stages of the transmitter. Output stages will be looked upon in more detail in chapter 6.

3.2.1   Source Followers

Source followers were used after the oscillators as part of the output stage of the transmitter in order to provide adequate current to be able to drive the 50 Ω output load. It is therefore used at the very last part of the output stage.
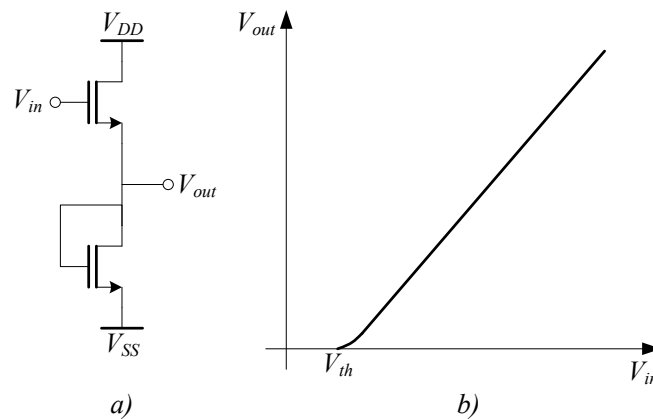
Figure 3.3: a) Circuit schematic and b) VTC of a source follower.

Source followers or common-drain amplifiers have a large current gain and a low output resistance but they suffer the disadvantage of dependence on body effects. This happens because the source is the output node therefore making the threshold voltage increase with the output, which means that the maximum output will be lower than V_{DD} [12].

From the voltage transfer characteristics(VTC) in fig. 3.3 it can be deduced that the signal input to the source follower must have $V_{in} > V_{th}$ for the transistor to operate. The output voltage will then *follow* the input voltage with a DC voltage offset equal to V_{GS} according to this equation

$$V_{out} = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{in} - V_{th} - V_{out})^2 R_{eq} \qquad (3.1)$$

where R_{eq} is the equivalent resistance due to the diode-connected load. The voltage gain can be calculated by differentiating the previous equation w.r.t.

V_{in}.

$$\frac{\partial V_{out}}{\partial V_{in}} = \mu_n C_{ox} \frac{W}{L}(V_{in} - V_{th} - V_{out})(1 - \frac{\partial V_{th}}{\partial V_{in}} - \frac{\partial V_{out}}{\partial V_{in}}) \tag{3.2}$$

and we can substitute in the equation using the following relation:

$$g_m = \mu_n C_{ox} \frac{W}{L}(V_{in} - V_{th} - V_{out}) \tag{3.3}$$

therefore the voltage gain (A_v) is given as follows:

$$A_v = \frac{g_m R_s}{1 + (g_m + g_{mb})R_s} \tag{3.4}$$

3.2.2 CML Amplifier

Differential amplifiers are required for use after circuits with differential signals such as oscillators designed in this work. Besides being used as buffers for isolating the oscillator from the load, differential amplifiers are also used in constructing the amplitude control unit, as explained later in chap. 6.
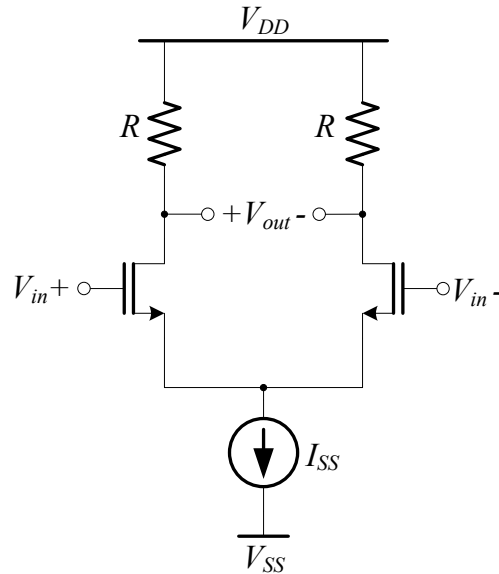
Figure 3.4: Schematic of a basic differential amplifier.

Current mode logic (CML) amplifiers, which are simply called differential pairs, provide a method for amplifying a differential signal. They consist of two common-source stages with their sources connected together. To reduce the sensitivity on the input common-mode voltage level ($V_{in,CM}$), a current source is

added as it is made clear in fig. 3.4. $V_{in,CM}$ is also important in that it determines the biasing of the transistors as well as the output signal levels, it is important to take care not to have a very large $V_{in,CM}$ to avoid clipping of the output signal. For the circuit in fig. 3.4 the current flowing in each transistor is $\frac{I_{SS}}{2}$, making the output common mode level equal:

$$V_{out,CM} = V_{DD} - \frac{I_{SS}}{2}R_S \tag{3.5}$$

which is independant of $V_{in,CM}$.

When designing such an amplifier, the two design considerations taken into account are: the mentioned common-mode constraints, to make sure that the signal does not undergo clipping, and the voltage gain, which is the main design feature of an amplifier. It is now useful to evaluate that voltage gain in terms of the design parameters. To start with, here is the expression for the input differential voltage.

$$V_{id} = V_{in1} - V_{in2} = V_{GS1} - V_{GS1} \tag{3.6}$$

and we assume that the devices are correctly biased for operation in saturation region, therefore the current is given by:

$$I_{DS} = \frac{1}{2}\mu_n C_{ox} \frac{W}{L}(V_{GS} - V_{th})^2 \tag{3.7}$$

therefore,

$$V_{GS} = \sqrt{\frac{2I_{DS}}{\mu_n C_{ox} \frac{W}{L}}} + V_{th} \tag{3.8}$$

From the previous two equations it follows that:

$$V_{in1} - V_{in2} = \sqrt{\frac{2I_{DS1}}{\mu_n C_{ox} \frac{W}{L}}} - \sqrt{\frac{2I_{DS2}}{\mu_n C_{ox} \frac{W}{L}}} \tag{3.9}$$

Then by squaring both sides and substituting $I_{DS1} + I_{DS2} = I_{SS}$ the following equation is result:

$$\frac{1}{2}\mu_n C_{ox} \frac{W}{L}(V_{in1} - V_{in2})^2 - I_{SS} = -2\sqrt{I_{DS1}I_{DS2}} \tag{3.10}$$

Squaring both sides again and using the equivalence of:

$$4I_{DS1}I_{DS2} = (I_{DS1} + I_{DS2})^2 - (I_{DS1} - I_{DS2})^2 = I_{SS}^2 - (I_{DS1} - I_{DS2})^2 \tag{3.11}$$

the following equation for differential current is arrived at, after re-taking the square root, then substituting $I_{DS1} - I_{DS2} = I_{out}$:

$$I_{out} = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}V_{id}\sqrt{\frac{4I_{SS}}{\mu_n C_{ox}} - V_{id}^2} \qquad (3.12)$$
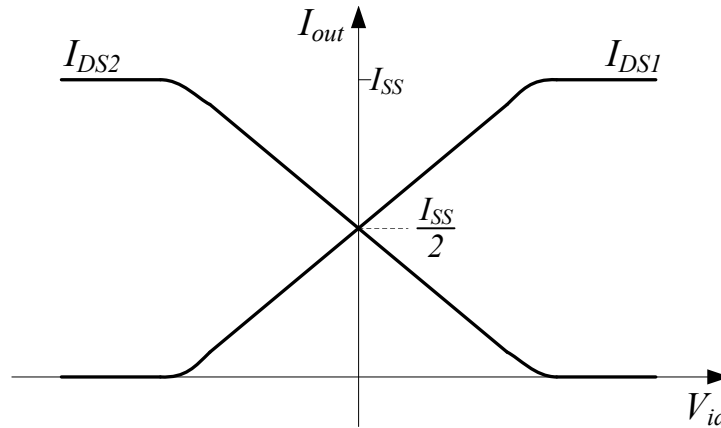
Figure 3.5: I_{out} vs. V_{id} for a differential amplifier.

The voltage gain is obtained from eqn. 3.12 at $V_{id} = 0$:

$$A_v = \sqrt{\mu_n C_{ox}\frac{W}{L}I_{SS}}R \qquad (3.13)$$

The degrees of freedom are therefore the transistors' sizes ($\frac{W}{L}$), the tail current (I_{SS}) and the load resistance (R) in controlling the gain. All the mentioned variables increase the gain with the largest effect through the load resistance since it is not under the square root.

3.3   Noise filters

An issue in most electronic circuits is its sensitivity to noise: how vulnerable a circuit is in response to noise present within it. In all cases it is an undesirable parasitic and can be avoided through the use of noise filtering techniques, one of which is presented in this section.

3.3.1   Low Pass RC filters

Oscillators with high tuning sensitivity achieve a wide tuning range, but the downside is that the frequency becomes prone to large variations through noise

on the tuning control inputs. This is avoidable only by reducing the noise on the tuning control inputs, and that is achieved by using RC low-pass filters.
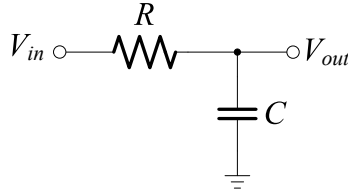
Figure 3.6: Low pass RC filter.

Thr RC series circuit shows low pass frequency response, which can be understood intuitively since the capacitor to ground will not affect low frequency (LF) signals while allowing HF signals to pass through to ground, hence allowing only the LF signals(in this case DC tune controls) to pass through to the circuit. It can also be proven from circuit analysis: the total impedance of series RC is:

$$Z_{eq} = R + \frac{1}{sC} \tag{3.14}$$

the transfer function for V_{out} can be therefore calculated as the ratio of the capacitor impedance to the total impedance as follows:

$$\frac{V_{out}}{V_{in}} = \frac{1/sC}{R + 1/sC} \tag{3.15}$$

$$= \frac{1}{1 + sCR} \tag{3.16}$$

This transfer function will yield transfer characteristics like those shown in fig. 3.7 with the cut-off frequency $f_c = \frac{1}{2\pi\sqrt{RC}}$. This frequency can therefore be chosen using the values of R and C to best suit the noise frequencies that need to be filtered out.

3.3.2 Noise Filtering on Supply Rail

Noise is not only a problem on the tuning inputs but on the supply rail as well. The oscillator frequency varies with the supply voltage, an effect known as *frequency pushing*. It is of high importance to avoid this problem especially in circuits where the supply voltage is unstable and prone to change. It can also be observed from the supply current, if it has many fluctuations then the circuit would most probably need more effective noise filtering, as was observed with ring oscillators.
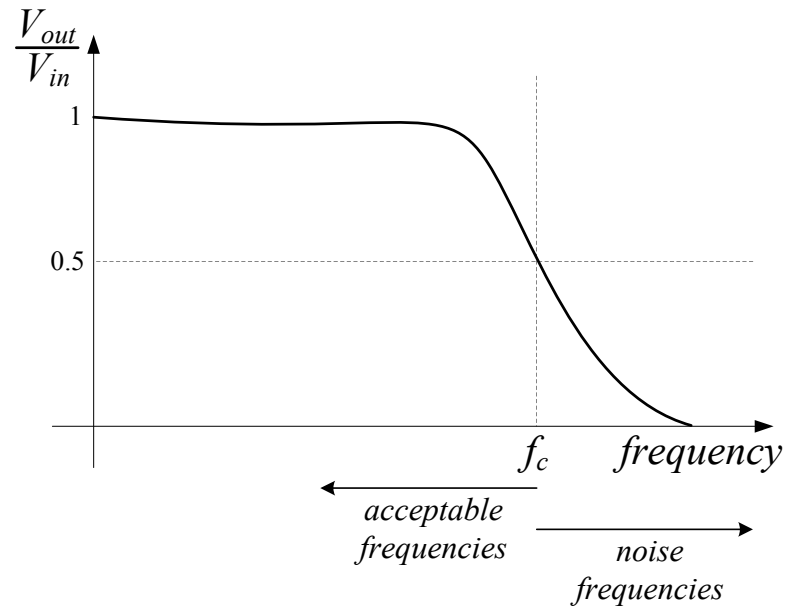
Figure 3.7: Low pass filter frequency response.

MOS capacitors were placed between the supply rail lines, this is done, for the case of n-channel transistors, by connecting the gate to V_{DD} and the source, drain and bulk to V_{SS} therefore having an equivalent capacitance equal to the oxide capacitance which increases noise immunity.
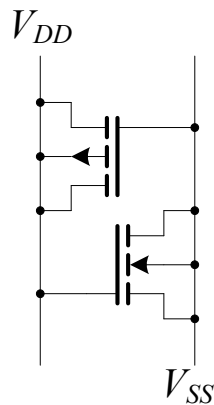
Figure 3.8: MOS capacitors between supply rail to reduce noise.

3.4   LC Resonators

Resonance occurs naturally in many systems, any system that has a complex conjugate pair of poles [13]. They are characterized by a sharp peak in the amplitude of their response corresponding to a phase of zero in their output. An LC resonator is the core component of an LC oscillator as will be shown in chapter 4. The frequency selectivity of such circuits is the reason they are suitable for use in transmitters, they are also used in filters as part of receivers.
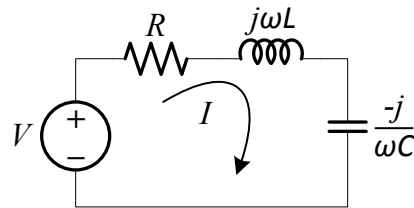
Figure 3.9: Series RLC circuit.

The resonance condition occurs when the capacitive and inductive reactances are equal in magnitude, thereby yielding a purely resistive impedance.

Considering the series RLC circuit in fig. 3.9, the input impedance is

$$Z = R + j\omega L + \frac{1}{j\omega C} \tag{3.17}$$

which can also be written in the following form:

$$Z = R + j(\omega L - \frac{1}{\omega C}) \tag{3.18}$$

It is therefore obvious that there exists a frequency ω for which the imaginary portion of the impedance cancels out, this is called the resonant frequency ω_0 and can be found as follows,

$$Im(Z) = \omega L - \frac{1}{\omega C} = 0 \tag{3.19}$$

therefore,

$$\omega_0 = \frac{1}{\sqrt{LC}} \tag{3.20}$$

At the obtained resonant frequency, the following is true for the resonant RLC circuit.

1. The circuit impedance is purely resistive since the reactances of the inductor and capacitor cancel out.

2. Impedance is at a minimum magnitude value.

3. The voltage and current are in phase, also because the equivalent impedance is resistive.

4. The reactive components' voltages can exceed the power supply voltage.

The discussed circuit is already acting as a frequency filter which can be seen from the frequency response shown in fig. 3.10. A *bandwidth* for the system can be defined as the difference between the two frequencies $\omega_2 - \omega_1$ which are defined at $\frac{1}{2}$ maximum power or $\frac{1}{\sqrt{2}}$ of the maximum current. Note that this is only one definition of bandwidth (BW).
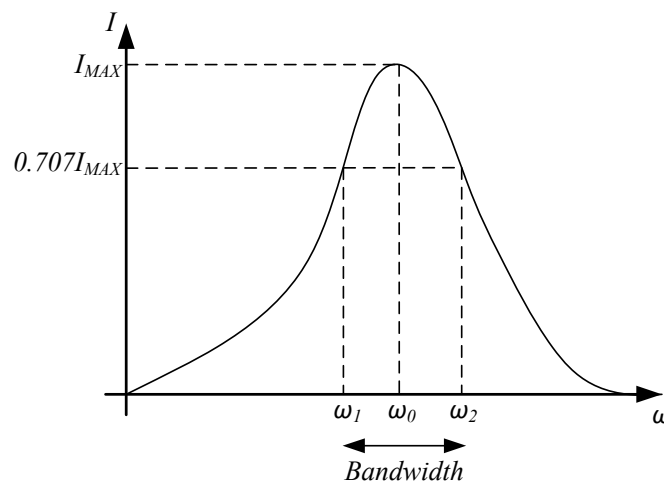
Figure 3.10: Current amplitude as it varies with frequency in a series resonant circuit.

ω_1 and ω_2 are called the half-power frequencies, an expression for calculating them can be obtained by equating the magnitude of the expression for impedance to $\frac{R}{\sqrt{2}}$ since it is this value at which the current drops to $\frac{I_{max}}{\sqrt{2}}$. By doing so, we arrive at the following expressions for the half-power frequencies

$$\omega_{1,2} = \pm\frac{R}{2L} + \sqrt{(\frac{R}{2L})^2 + \frac{1}{LC}} \tag{3.21}$$

It can be proven that the resonant frequency is the geometric sum of the two half-power frequencies [13].

$$\omega_0 = \sqrt{\omega_1\omega_2} \tag{3.22}$$

A very important parameter that is calculated for resonant circuits, and is of high relevance to oscillators, is the circuit's quality factor. It is defined as the ratio of the peak energy in the system and the energy dissipated in one cycle of oscillation at resonance. It is also regarded as a measure of *energy storage* property of the circuit with regard to its *energy dissipation* property [13].

The energy stored in the circuit per period is

$$P_{stored} = \frac{1}{2} L I^2 \tag{3.23}$$

and the energy dissipated in the resistor is equal to

$$P_{dissipated} = \frac{1}{2f} I^2 R \tag{3.24}$$

therefore the quality factor is the ratio of both multiplied by 2π,

$$Q = \frac{\omega_0 L}{R} = \frac{1}{\omega_0 C R} \tag{3.25}$$
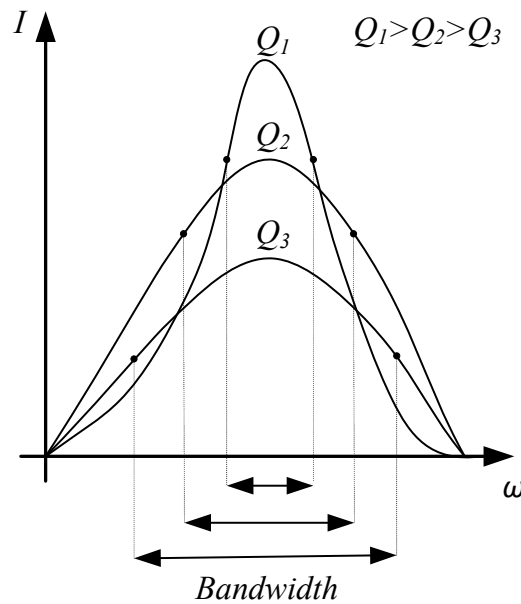
Figure 3.11: Current amplitude as it varies with frequency for different Q's.

The quality factor describes the *sharpness* of the amplitude curve in the frequency response, therefore it makes sense to relate it to the bandwidth. Q is inversely proportional to the bandwidth since the more sharp the amplitude curve gets, the narrower it will be as well, making the BW decrease. This is

illustrated by the plots in fig. 3.11. By substitution using eqn. 3.21 and the definition $BW = \omega_2 - \omega_1$,

$$BW = \frac{R}{L} = \frac{\omega_0}{Q} \tag{3.26}$$

The quality factor describes the selectivity of the circuit; the ability of the circuit to work at a specific frequency and reject the other frequencies. This is why, as we will see later, Q of the used passive elements are directly related to an oscillator's phase noise performance. High Q resonators are desired for use in modern communication devices.
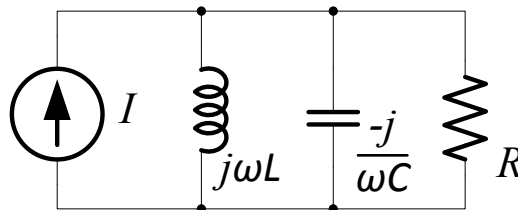
Figure 3.12: Parallel RLC circuit.

All the previous analysis was done on series RLC circuits, it remains to look at how the parallel RLC circuits behave. There are four parameters that characterize resonant circuits and they are ω_0, Q, BW and half power frequencies. They can be found for parallel RLC circuits the same way as for the series ones, and here are their expressions.

$$\omega_0 = \frac{1}{\sqrt{LC}} \tag{3.27}$$

$$Q = \omega_0 RC = \frac{R}{\omega_0 L} \tag{3.28}$$

$$BW = \frac{1}{RC} = \frac{\omega_0}{Q} \tag{3.29}$$

$$\omega_{1,2} = \pm\frac{R}{2RC} + \sqrt{(\frac{R}{2RC})^2 + \frac{1}{LC}} \tag{3.30}$$

This concludes the section about LC resonators. They are the basic building block on which LC oscillators are built, the idea is to compensate for a lossy LC tank by using an active circuit to cancel out the parasitic resistance introduced from the passive components. This is discussed in detail in chapter 4, along with another look at LC resonators from the point of view of the oscillators in which they are used.

Chapter 4

Oscillators

The design of an oscillator is unique, different from any other electronic circuit. An oscillator is a circuit that produces a periodic output voltage without any external inputs by relying on unstable operation. Instability, which is usually avoided in any other system, must be applied here, but carefully controlled in order to get an output suitable for use in modern high-performance RF receivers and transmitters, which are demanding in terms of power consumption, spectral purity and amplitude stability.

In this chapter, the general conditions for oscillation in a given system are presented, followed by a survey of different oscillator topologies, with focus on ring-oscillators and LC oscillators. A lot of the text in this chapter is the result of studying the equivalent chapter in [5].

Note that in oscillators a very important property is phase noise performance, but because this work is only a first prototype for the used technology, it is not of high importance to investigate this point which is why this document does not include the relevant phase noise theory or simulations.

4.1   Oscillation Conditions

Oscillation conditions for a feedback system can be summarized in two necessary criteria [5, 14]:

- Open loop gain of the system is greater than 1.

- Phase shift caused by the system is 180°.

This is further clarified with the aid of fig. 4.1. The system shown in the figure consists of a subtractor (negative feedback), and a block specifying any certain function denoted by H(s). Consider the input at the first step in fig. 4.1, assuming the system has no initial conditions at the feedback, the input will
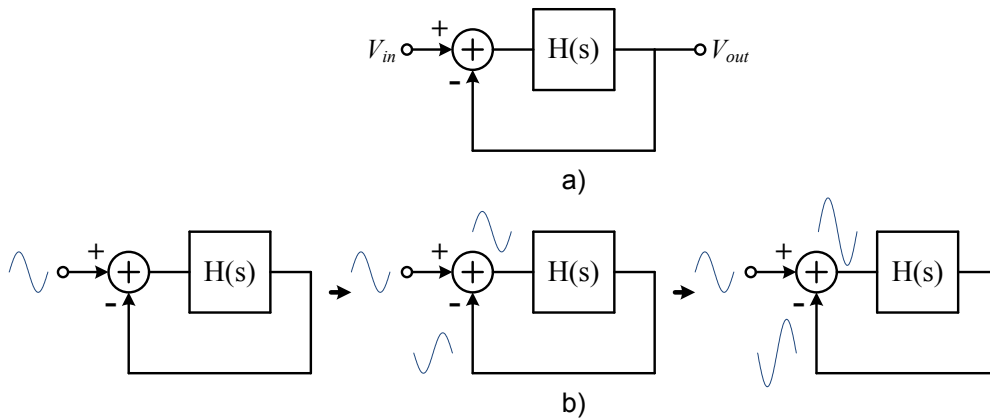
Figure 4.1: a)Feedback system, b)Instability in an oscillatory system.

enter through the subtractor, then onto the H(s) block unchanged. At this point, if oscillation would continue to occur, then the output of H(s) must add up to the input, and for that to occur it must be out of phase with it (since there is a subtractor) hence the second condition. The feedback system must provide 180° ($\pm 360°n$) to add up to the input and sustain oscillation. Note that a complete phase shift of 360° is achieved around the system when the subtractor's phase shift is also taken into account.

The other condition states that the loop gain must be greater than or equal to 1, indicating that some kind of amplification is required. This can be clarified by following the waveform around the system, which leads to the following geometric series:

$$V_{out} = V_{in} + |H(s)|V_{in} + |H(s)|^2 V_{in} + |H(s)|^3 V_{in} + \cdots \tag{4.1}$$

which can be written in the closed form (for $|H(s)| \leq 1$):

$$\frac{V_{out}}{V_{in}} = \frac{1}{1 - |H(s)|} \tag{4.2}$$

so this clearly only diverges for values of $|H(s)|$ that are greater than or equal to 1.

These conditions stated above are known as the "Barkhausen criteria" and can be formally summarized in the following two equations:

$$|H(s)| \geq 1 \tag{4.3}$$

$$\angle H(s) = 180° \tag{4.4}$$

To be safe, the loop gain is usually chosen to be 2 or 3 times the required value, depending on the system, in order to assure oscillation in spite of temperature variations or other external variables.

4.2 LC Oscillators

As the name suggests, LC oscillators depend on resonance from an LC tank to satisfy oscillation conditions, namely, the "Barkhausen Criteria" mentioned earlier. Had there been ideal capacitors and inductors, it would have been trivial to construct an LC oscillator, since it will be sufficient to place a capacitor and an inductor in series or parallel form. Upon injecting some energy into the system at its center frequency; the impedance will amount to zero and energy will be indefinitely transferred from the capacitor to the inductor, or *oscillate* between them. Of course this is not the case.

4.2.1 LC Resonators

Integrated capacitors and monolithic inductors have been available on-chip for more than 15 years [5], a detailed account of these components is given in chapter 2. Inductors are usually the performance limiting components due to their low quality factors when implemented on-chip in integrated form. They usually exhibit low quality factors (< 10), indicating that the *oscillating energy* is no longer sustained, rather dissipated in a resistive component.
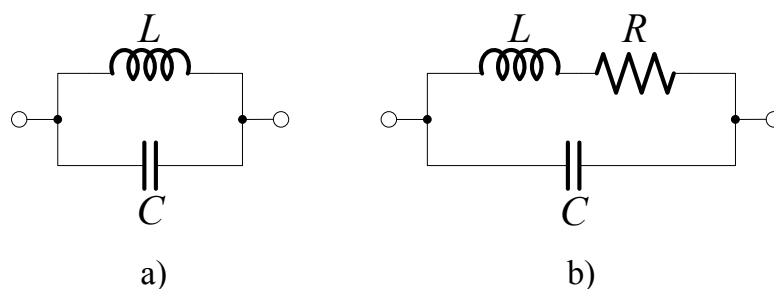
Figure 4.2: a)Lossless and b)realistic parallel LC resonator.

In the ideal case the combined impedance of the parallel resonant tank can be given by: $Y_{eq} = \frac{1}{j\omega L} + j\omega C$, which reduces to zero ($Z_{eq} = \infty$), at $\omega = \omega_0 = \frac{1}{\sqrt{LC}}$, thereby yielding an infinite Q at this resonant frequency [5]. This is the case when the energy initially stored in one of the components will not be dissipated, only being transferred back and forth within the LC tank.

Impedance of the lossy tank is given as:

$$Z_{eq} = \frac{Ls + R}{LCs^2 + RCs + 1} \tag{4.5}$$

In the vicinity of the resonant frequency ω_0, but not at exactly ω_0, the tank reduces to a simple resistor, the exact resonant frequency is a complicated function of R. The insight gained here is that the tank no longer has an infinite Q, rather a finite one, given by: $Q = \frac{\omega L}{R}$. At resonance, energy will still be transferred between the reactive elements at the speed specified by the natural frequency of the system, but since the energy will pass through a resistor on each cycle, any waveform present will eventually die out without external stimulus.

a)

b)
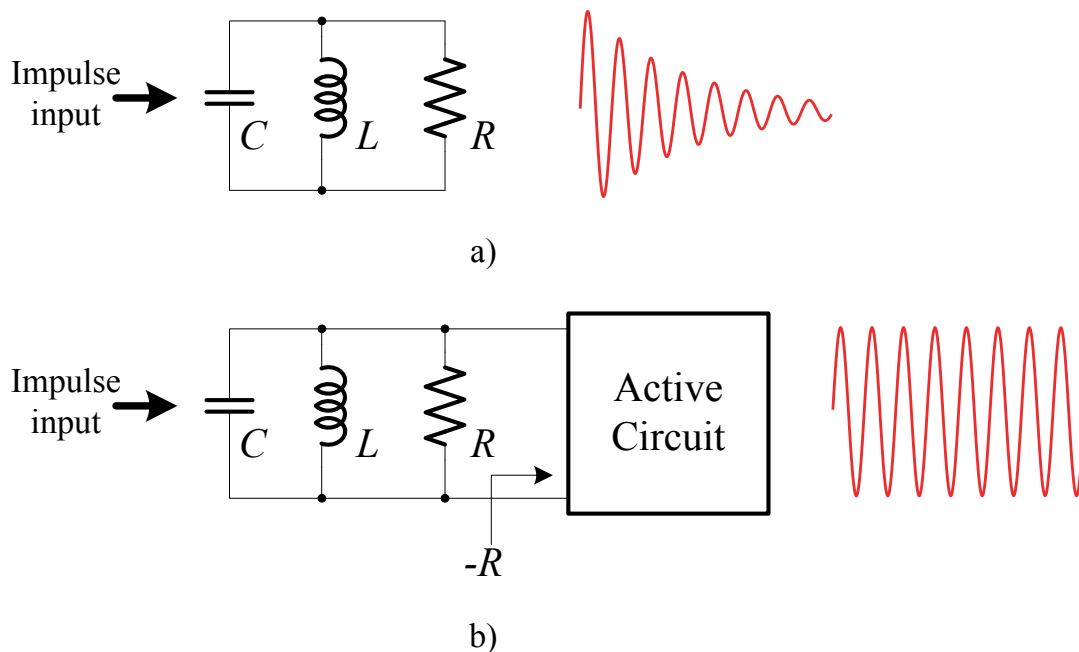
Figure 4.3: a)Decay of oscillation signal due to resistive loss. b)Use of an active circuit to compensate for loss and sustain oscillation.

It is now the job of the circuit designer to design some kind of active circuitry that will compensate for the power lost in the resistor by acting as *negative resistance* as clarified in fig. 4.3, or by amplifying the signal enough within one cycle to be able to keep the oscillation going.

From the point-of-view of the "Barkhausen Criteria", we see from fig. 4.4 that the phase of an LC tank already satisfies the second criterion. The loop gain is 0°, that is, the oscillating waveform will *add up* each oscillation cycle. It remains now to investigate the condition imposed on the gain; it must be greater than 1. As mentioned earlier, this will be the job of an active circuit.
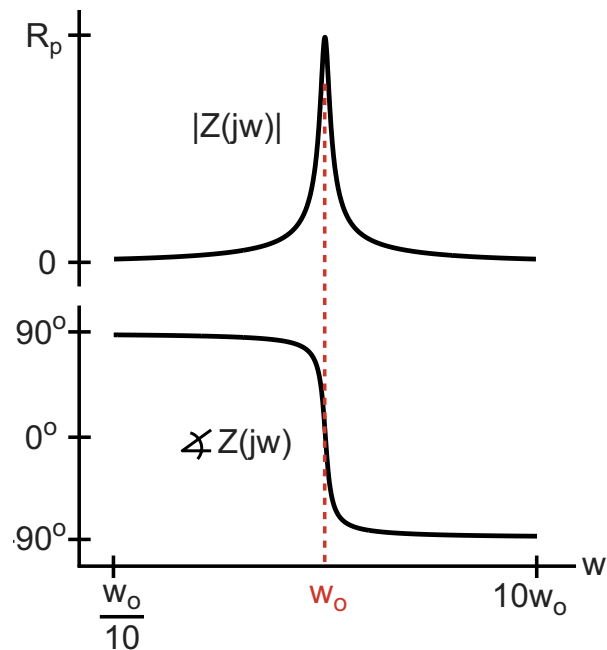
Figure 4.4: Magnitude and phase of the impedance of a lossy resonant LC tank [2].

4.2.2   Cross-Coupled Oscillators

The first LC oscillator topology to be discussed is the crossed-coupled oscillator which utilizes negative resistance, in form of a cross-coupled transistor pair, to cancel out the losses created by the LC tank parasitic resistance.

As shown in fig. 4.5 the architecture of this type of oscillator is quite simple, it consists of an LC tank with NMOS, and optionally PMOS, negative transconductance components as the cross-coupled pairs shown in the figure.

It is now instructive to examine how the shown circuitry can provide the so called *negative resistance*. To get an idea how negative resistance (or negative transconductance) can be realized, one can go back to the definition of resistance which is the change of voltage divided by the change in current at a given point. This indicates that if increase in voltage causes decrease in current at any point, the resistance at this point should be negative. In terms of system attributes, the open-loop gain of the system must be negative to have negative resistance [5].

With reference to fig. 4.6 the outcome of negative resistance from the NMOS cross-coupled pair will be proved. In the same figure is the circuit replaced by
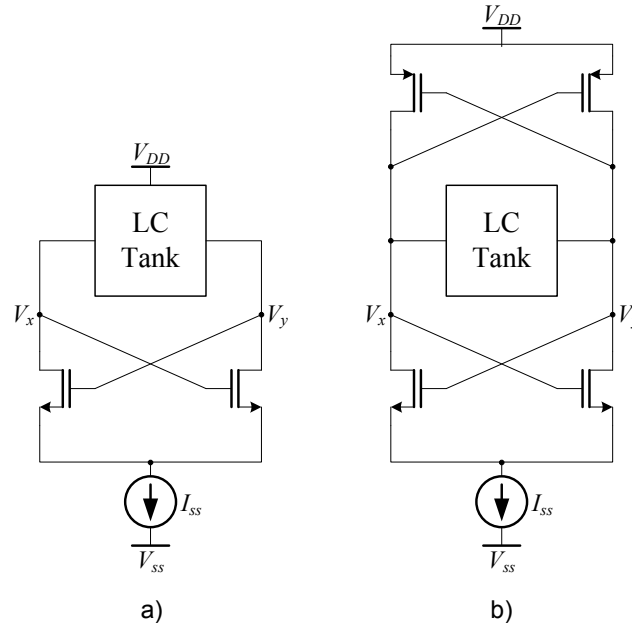
Figure 4.5: Abstract circuit diagram of cross-coupled oscillator with a) NMOS cross-coupling, b) both NMOS and PMOS cross-coupling.

the small signal model to facilitate analysis.

$$I_x = -g_{m1}V_1 = g_{m2}V_2 \tag{4.6}$$

$$V_x = V_1 - V_2 \tag{4.7}$$

$V_1 = -\frac{I_x}{g_{m1}}$ and $V_2 = \frac{I_x}{g_{m2}}$ therefore,

$$V_x = -\frac{I_x}{g_{m1}} - \frac{I_x}{g_{m2}} \tag{4.8}$$

and if $g_{m1} = g_{m2} = g_m$,

$$\frac{V_x}{I_x} = -\frac{2}{g_m} \tag{4.9}$$

Therefore a negative resistance of $Z = -\frac{2}{g_m}$ will be connected in parallel to the LC tank, and assuming the resistance of the resonator is R, the condition imposed when designing the cross-coupled pair is:

$$Z = R \parallel -\frac{2}{g_m} \tag{4.10}$$
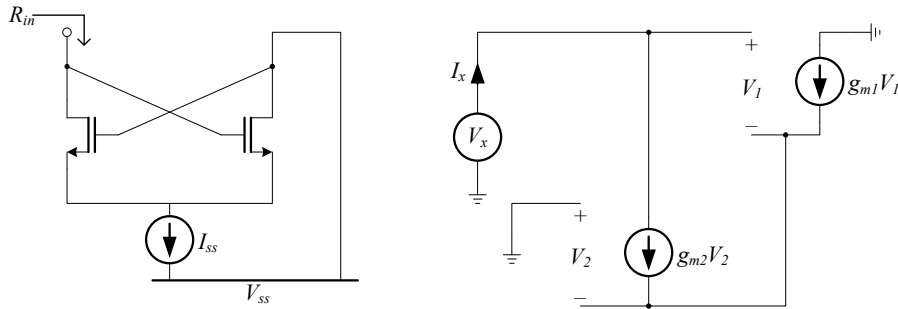
Figure 4.6: Cross-coupled NMOS transistor pair and the small signal model equivalent.

$$Z = \frac{1 - g_m R}{2R} \tag{4.11}$$

and a negative overall resistance is required, therefore,

$$R \geq \frac{2}{g_m} \tag{4.12}$$

From the previous set of equations it is deduced that when $R \geq \frac{2}{g_m}$ the inductor's losses are cancelled and oscillation should sustain in a cross-coupled oscillator.

Previously, the cross-coupled oscillator is proved to provide negative resistance, and therefore sustain oscillation, from the circuits point of view. Another approach to reach the same conclusion is presented in [2], where the system is considered rather than the circuit, and it is represented by a block diagram, shown in fig. 4.7. Since $Z(j\omega)$ is supposedly purely real at resonance, g_m should also be so to fulfill phase conditions [2].

Root loci of the system are shown at different values of gain in fig. 4.8. It restates what has already been proved by circuit analysis; that the system will continue to oscillate only if $g_m R \geq 1$, which is the same as the condition derived in eqn. 4.12 (without the factor of 2 since here R_p is actually twice "R" that is used in the derivation).

From the root-locus plots, there are three cases to be distinguished: the first is when $g_m R < 1$, in this case the overall real part of the system impedance is positive and oscillation cannot continue in the system since its is *damped* by power dissipation in the resistance. The second case is when $g_m R = 1$ exactly, this means that the negative resistance exactly matches the parasitic resistance in the system cancelling out any real part of the impedance and allowing oscillation
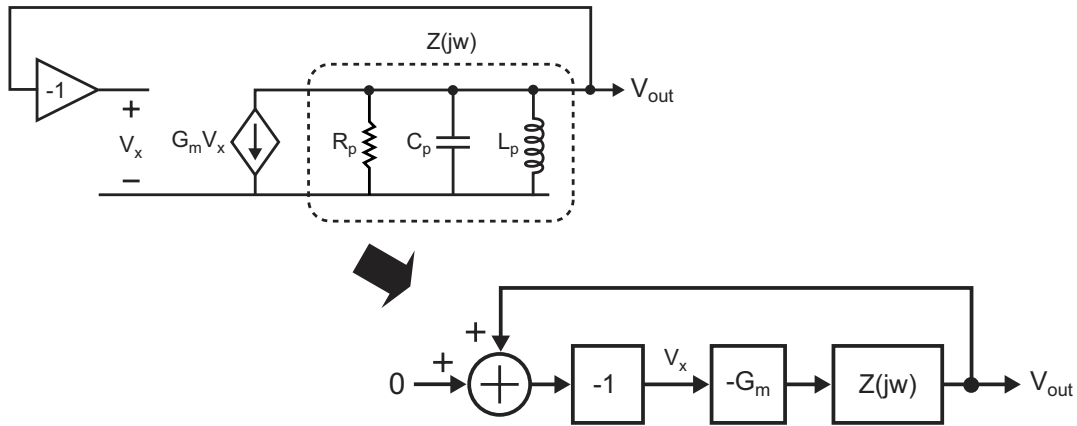
Figure 4.7: Block diagram describing cross-coupled oscillator [2].

to proceed. The third case is when the parasitic resistance is overcompensated by the negative transconductance therefore there is a net amplification in the system and this is why the waveform appears to be growing indefinitely. In reality, of course, the signal will saturate at the upper limit of V_{DD} and the lower limit of V_{SS}.

4.2.3   Colpitts and Other LC Oscillators

Colpitts oscillators are named after their developer, so are many other oscillators as well. Its principle of operation is quite similar to that of the crossed-coupled oscillators; there is also a negative resistance component that is used to cancel out the parasitic resistance presented by the LC resonator.

Referring to fig. 4.9, it is easy to see how negative resistance is utilized in order to construct the oscillator. It is also shown how the basic circuit looks like after proper biasing is added. Note that an additional capacitor is connected from the transistor's source terminal to ground because if this is not present the impedance from this node to ground would be infinite [5].

Here is a proof that the circuit in fig. 4.9 actually simulates a negative resistance component, assuming that the voltage and current at the input port (clarified by an arrow) are V_x and I_x respectively. By performing Kirchoff's voltage law for circuit analysis (summing up the voltages around a loop):

$$V_x = \left(I_x - \frac{-I_x}{C_1 s} g_m \right) \frac{1}{C_2 s} + \frac{I_x}{C_1 s} \tag{4.13}$$
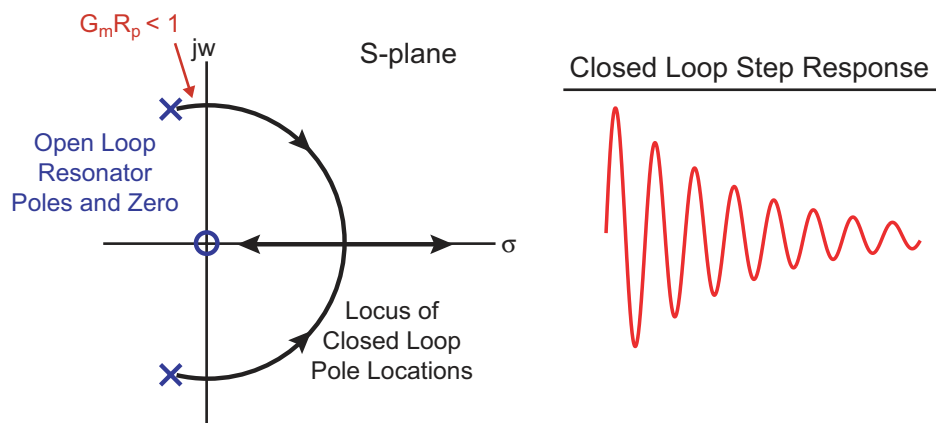
(a)
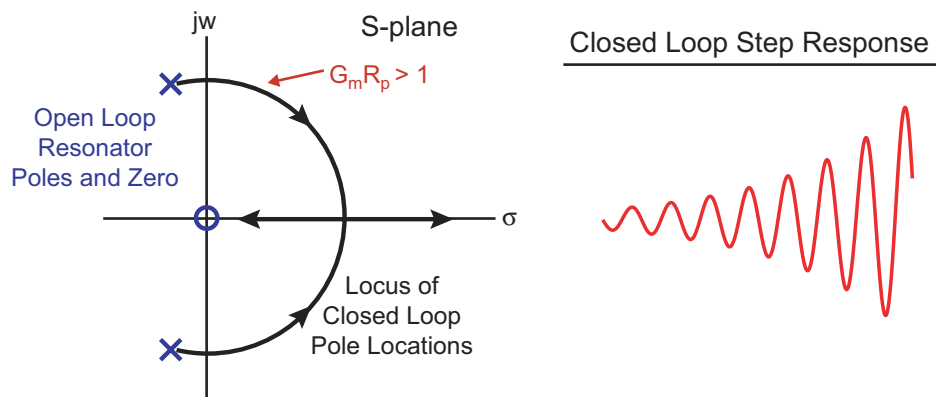
(b)
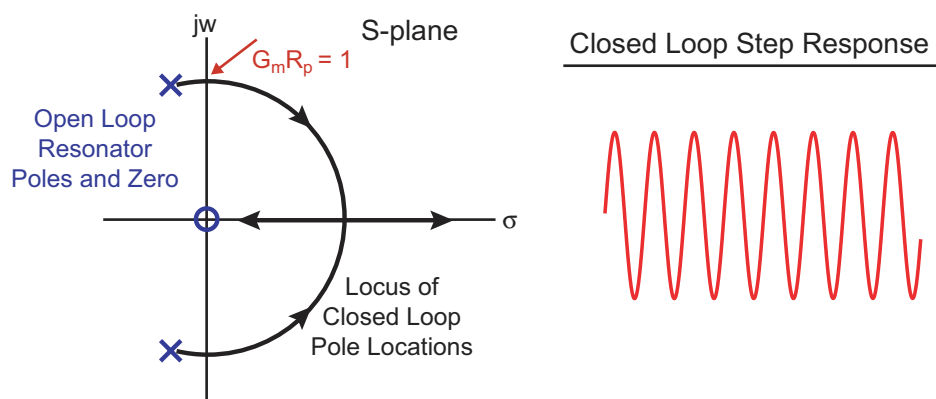
(c)

Figure 4.8: Root loci of cross-coupled oscillator showing the effect of different values of $g_m R$ [2].
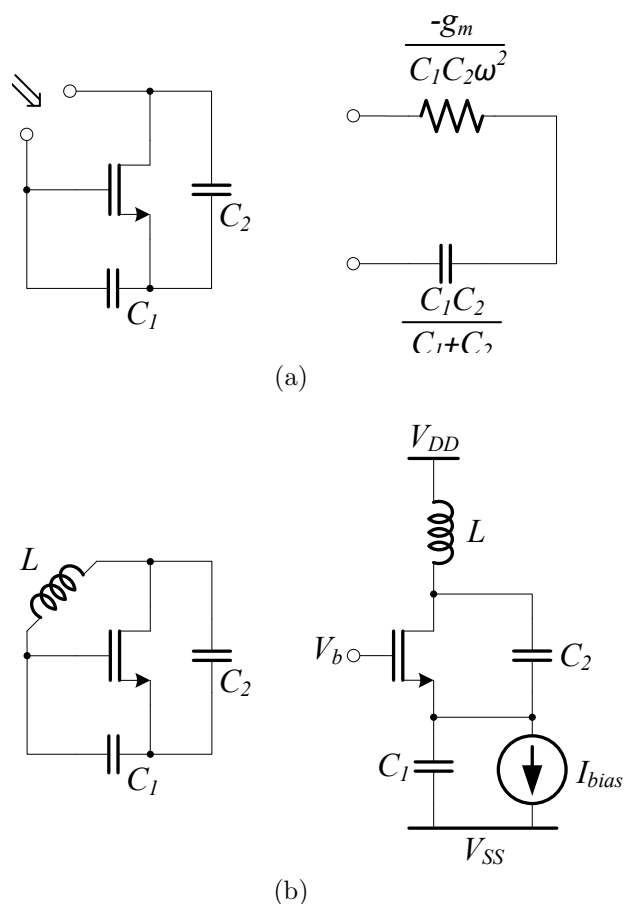
Figure 4.9: a) Negative resistance used in the Colpitts Oscillator. b) Colpitts oscillator shown using proper biasing.

and therefore,

$$Z_{eq} = \frac{V_x}{I_x} = \frac{g_m}{C_1 C_2 s^2} + \frac{C_1 C_2}{s(C_1 + C_2)} \tag{4.14}$$

the equivalent impedance after substituting $s = j\omega$ is thus separated into the following resistance and capacitance placed in series:

$$R_{eq} = -\frac{g_m}{C_1 C_2 \omega^2} \tag{4.15}$$

$$C_{eq} = \frac{C_1 C_2}{C_1 + C_2} \tag{4.16}$$

It is important to go back to the "Barkhausen Criteria" once more and investigate how they apply on the Colpitts circuit, starting with the phase condition.

The oscillator, as can be seen in its schematic, is in common-source topology meaning that the phase shift between input and output (the gate and drain) is 180°. This part can be thought of as feed-forward or open loop circuit, and therefore 180° is the required phase shift here for oscillation.

Feedback is provided through capacitor C_2 (in fig. 4.9) and that is responsible for the negative feedback from drain to source. A capacitor exists in the feedback in order not to disturb the bias point of the transistor used [5].

Now that the phase conditions are satisfied for this circuit, it is left to look at the magnitude condition. And to do that, the circuit is analyzed in using its small-signal model as shown in fig. 4.10. The current through resistor is $\frac{V_{out}}{R}$ and through the inductor $\frac{V_{out}}{sL}$. The current through C_1 is equal to $I_{in} - I_{ind} - I_{res}$, and therefore:

$$V_1 = -(I_{in} - \frac{V_{out}}{Ls} - \frac{V_{out}}{R})\frac{1}{C_1 s} \tag{4.17}$$

and the current through C_2 can be written as $(V_{out} + V_1)C_2 s$. It remains to sum up all the currents at the output (using Kirchoff's current law for circuit analysis) and rearrange the equation in the following form

$$\frac{V_{out}}{I_{in}} = \frac{RLs(g_m + C_2 s)}{RC_1 C_2 Ls^3 + (C_1 + C_2)Ls^2 + [g_m L_p + R_p(C_1 + C_2)]s + g_m R} \tag{4.18}$$

The circuit will oscillate if the closed-loop transfer function (eqn. 4.18) goes to infinity when $s = j\omega_R$ [5]. For this to happen, the denominator's real and imaginary components must drop to zero, yielding the following conditions:

$$-RC_1 C_2 L\omega_r{}^3 + [g_m L + R(C_1 + C_2)]\omega_r = 0 \tag{4.19}$$

$$-(C_1 + C_2)L\omega_r{}^2 + g_m R = 0 \tag{4.20}$$

These two equations, under the valid assumption that $g_m L \ll R(C_1 + C_2)$ yield the following conditions:

$$\omega_r{}^2 = \frac{1}{L\frac{C_1 C_2}{C_1 + C_2}} \tag{4.21}$$

$$g_m R = \frac{C_1}{C_2}(1 + \frac{C_2}{C_1})^2 \tag{4.22}$$

To have the minimum required gain it can be proven that $\frac{C_1}{C_2} = 1$, this imposes the condition that:

$$g_m R \geq 4 \tag{4.23}$$

Recall previously, in the crossed coupled oscillator, that the value is only required to be greater than 1, which exposes a disadvantage of the Colpitts oscillator with respect to the cross-coupled one. This issue is decisive if the used inductor's quality factor is low and thus has a low value for R (note that R here represents the parallel resistance). In fact, the inductor usually is the design bottleneck and that is why the cross-coupled oscillators are more widely used, and the reason behind their use in this work as well.
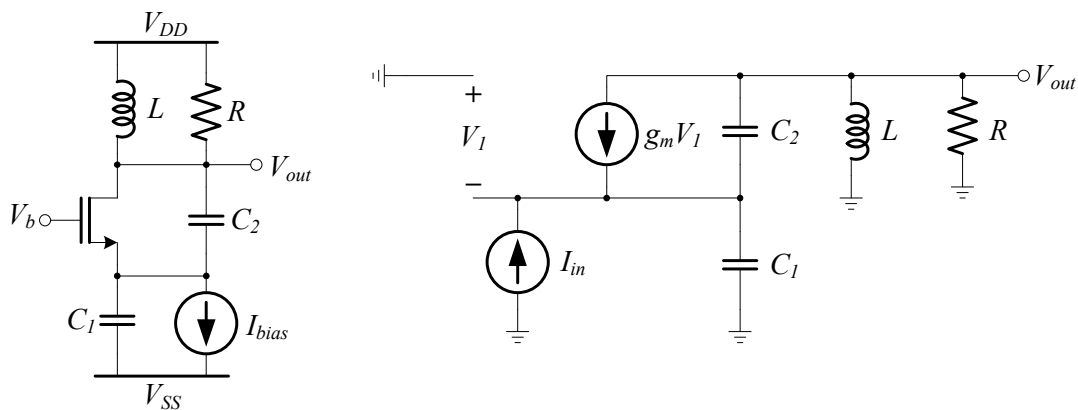
Figure 4.10: Colpitts oscillator and its small-signal equivalent model.

4.3   Ring Oscillators

Ring oscillators usually exhibit poor noise performance and output a signal with poor spectral purity, this is why it is usually unfavored in use of modern RF devices. It usually does not meet the specifications. They are, however, easier to integrate in today's CMOS technology due to the absence of monolithic inductors, and usually have a much smaller area for the same reason. It is found as well that a wide tuning range is easier to obtain in ring oscillators than it is in LC oscillators.

The principle of operation of ring oscillators is very simple to grasp; it consists of an odd number of inverter gain stages which constantly invert the signal resulting in oscillation. The frequency of oscillation depends on the delay of each inverter and the presence of capacitors between the inverters.

Revisiting the "Barkhausen criteria", and specifically the phase condition, it is found that only ring oscillators of odd number of stages will oscillate, and they must be greater than 1 stage as well, since the total phase shift around the system must be 360°. Referring to fig. 4.11 for clarity, we find that when there

is only 1 stage, the total phase shift is 270° since the inverter stage provides 180° and the single pole (due to the capacitor) a further 90° [5]. The two stage chain can never oscillate either, intuitively it can be deduced that the circuit will *latch-up* because one stage will continue to output a high voltage, until it reaches V_{DD} while the other will have high voltage at the input therefore the output will be low. This will continue until both inverters reach the power supply voltages. Another way of looking at it is through the phase shift; in the case of 2 stages, the total phase shift will be equal 360° at $\omega = 0$ and 180° at $\omega = \infty$, meaning it will not reach a multiple of 360° at any frequency between $\omega = 0$ and $\omega = \infty$, this violates the "Barkhausen Criteria".

The three stage chain, however, will oscillate due to the fulfillment of both the "Barkhausen Criteria", since it overcomes both the shortcomings displayed by the mentioned 1 and 2 stage chains. To start with, the phase condition is satisfied since the total phase shift will be 540° at $\omega = 0$ (due to 3 inverters each supplying 180°) and at $\omega = \infty$ it will reach 270° (due to an additional $-270°$ from the capacitors). It is now clear that at some frequency in between $\omega = 0$ and $\omega = \infty$ the total phase shift will be 360°. This is made clear in fig. 4.12
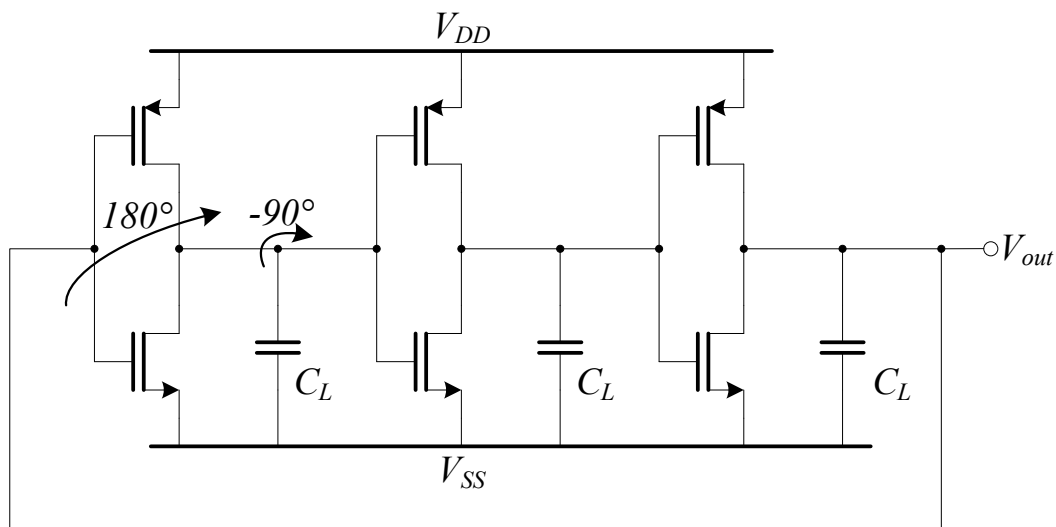
Figure 4.11: Three stage CMOS ring oscillator clarifying the sources of phase delay.

The capacitors between the inverter stages are always present due to parasitics, but when further slowing down of oscillation is required, they can be placed to control the frequency at which the ring oscillator functions.

With fig. 4.11 as the reference, small-signal analysis will be done on the ring oscillator to investigate oscillation criteria. It was already proven that the

phase criteria are fulfilled since there exists a frequency at which the loop gain is exactly 360°. It is now the challenge to assure that the loop gain exceeds 1 at this frequency in order to fulfill the magnitude condition. To start, here is the open-loop transfer function of the 3 pole system (assuming all stages are identical, where $\omega_0 = \frac{1}{RC}$):

$$H(s) = -\frac{A^3}{(1 + \frac{s}{\omega_0})^3} \tag{4.24}$$

The open loop transfer function of a negative feedback system should provide 180° of phase shift, indicating that each pole should provide that amount divided by 3, ie. 60° of phase shift (ϕ):

$$\phi = \tan^{-1}(\frac{\omega_{osc}}{\omega_0}) \tag{4.25}$$

$$\omega_{osc} = \omega_0\sqrt{3} \tag{4.26}$$

where the variable ω_{osc} is the oscillation frequency. Now the voltage gain per inverter stage must be so that $|H(j\omega)| \geq 1$ at the frequency calculated in eqn. 4.26 therefore:

$$\frac{A^3}{\sqrt{1 + (\frac{s}{\omega_0})^2}} \geq 1 \tag{4.27}$$

therefore,

$$A \geq 2 \tag{4.28}$$

to fulfill the magnitude criterion for oscillation. It is now left to analyze the system at different values of the mentioned gain. A plot of the root loci is shown in fig. 4.13 clarifying the behavior at different values of gain.

When the gain is below the required value, the poles of the system all reside in the left half plane which means that the system is stable and oscillation will keep decreasing. Mathematically one can think of it as a sinusoid multiplied by a decaying exponential factor arising from the real part in the poles' values. If the gain is exactly 2, the poles are situated exactly on the imaginary axis resulting in oscillatory behavior. Laplace transform when applied on purely imaginary poles will result in a sinusoidal function. The third case is when the poles are in the right half plane resulting in a positive exponential multiplied by a sinusoid which results in a growing waveform that saturates at V_{DD} and V_{SS} in a practical circuit.

The time domain transformation of the closed loop transfer function describing the ring oscillator system is derived in [5], it can be easily transformed by
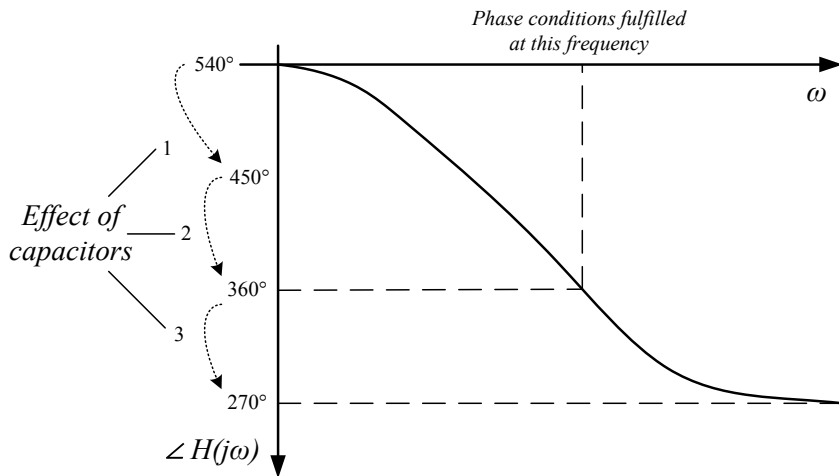
Figure 4.12: Phase plot for the 3-stage ring oscillator system.

obtaining the closed loop transfer function from the open loop one (in eqn. 4.24) it is:

$$V_{out}(t) = a\,exp(\frac{A_0 - 2}{2}\omega_0 t)cos(\frac{A_0\sqrt{3}}{2}\omega_0 t) \qquad (4.29)$$
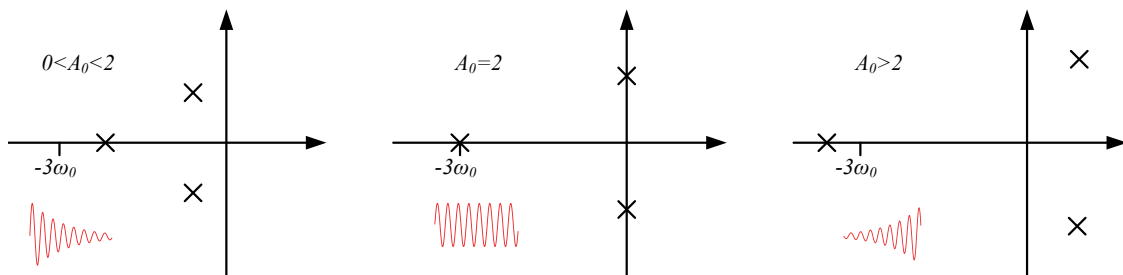
Figure 4.13: Poles for the ring oscillator at different values of gain.

The previous analysis is strictly small-signal and does not apply when the oscillator's voltage swing is from V_{DD} to V_{SS}, which is the case for CMOS-inverter based ring oscillators. In this case, large signal behavior must be taken into account, simply, by considering the delay of each inverter stage to find the frequency of oscillation. Fig. 4.14 clarifies this point. It shows the relationship between waveforms in a 3 stage ring oscillator taking the delay (T_D) of each stage into account.

When the first waveform drops from V_{DD} to V_{SS} it requires time=T_D for the signal at the following stage to rise, this delay is simply the inverter gate delay
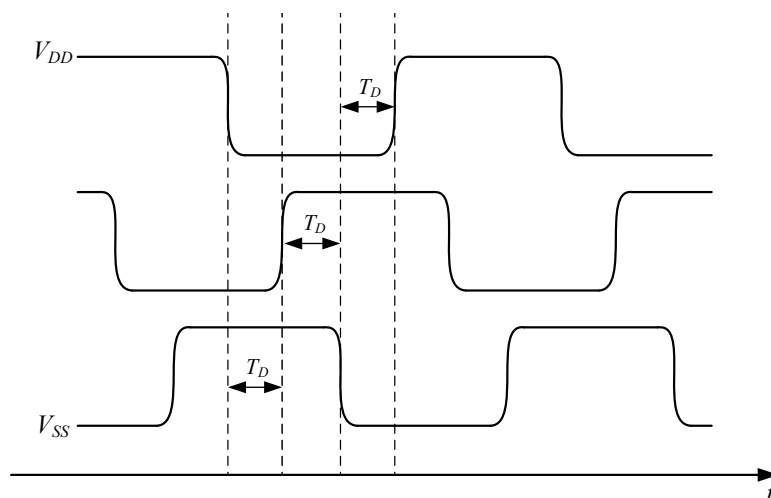
Figure 4.14: Waveforms after each stage in a ring oscillator.

and is related to the transit time of the transistor. The same is true for the signal at the output of the third inverter, consequently the period of oscillation is $6 \times T_D$. From here the frequency of oscillation equals $\frac{1}{6T_D}$, which is not necessarily equal to the previously calculated delay of $\frac{A_0\sqrt{3}\omega_0}{2}$. The question is: at which frequency does the system oscillate? The answer is intuitive: when oscillation starts, it is still small signal, and therefore oscillates at $\frac{A_0\sqrt{3}\omega_0}{2}$, but as oscillation grows and saturates at V_{DD}, it *shifts* to the other frequency of $\frac{1}{6T_D}$ which is slower [5].

Chapter 5

Voltage Controlled Oscillators

In modern telecommunications devices the frequency of operation is very tightly constrained to a specific frequency band, of small width, in order to accommodate for the various frequency bands nowadays. RFID systems are usually assigned frequencies in the international, scientific and medical bands (ISM) in which the allowed frequencies deviate from the center frequency by only about 2 MHz. In this chapter, an abstract model of a voltage controlled oscillator will be presented along with its system properties, followed by the discussion of tuning methods in LC and ring oscillators.

5.1   Introduction to VCOs

In an ideal case, the oscillating frequency of a transmitter would remain fixed at the center frequency used, however temperature and process variations affecting the transistor widths, carrier mobility and many other variables influence the frequency of operation causing unpredictable changes. The oscillator used in any transmitter is therefore usually frequency tunable through voltage or current in order to be able to *tune* the frequency back to the required center frequency.

An ideal VCO is a lossless block which has one (or many) input voltage which tunes the frequency of that block linearly. The system would be characterized by the following equation.

$$f_{out} = f_0 + K_{VCO}V_{cont} \tag{5.1}$$

Here the frequency is expressed as a function of the tuning sensitivity K_{VCO} and an initial offset frequency f_0 which is defined at zero tuning voltage. In the figure K_{VCO} has the units of Hz/V, since the tuning variable is voltage, but this must not always be the case, current could also be used to tune the frequency as it will also be shown in this work.

In fig. 5.1 the ideal and realistic transfer characteristics of a VCO are shown. It is usually the case that the curve contains non-linearities as shown in part b) of the same figure. The reason behind this is the dependence of frequency tuning on non-linear components, such as varactors or current steering, which also shows nonlinearities especially at the start and end of any given tuning range as shown.
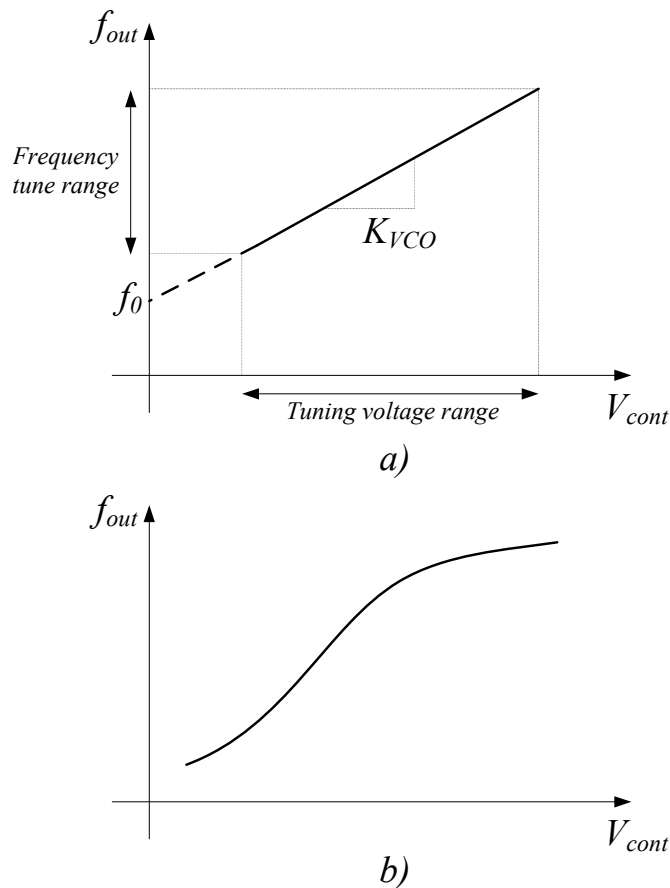
Figure 5.1: Transfer Characteristics of an a) ideal and b) realistic VCO.

The VCO is a system that contains attributes which usually define how suitable the designed circuit is for a specific application. As it is the case in many practical systems, the properties which will be discussed shortly trade-off with one another in a realistic VCO. After discussing the describing function of the VCO it is now best to summarize the main variables that characterize any VCO [5].

Center Frequency: This is the operating frequency of the oscillator which also coincides with a frequency within the specific frequency band used. This

should also be the value in the center of the frequency tune range in fig. 5.1.

Tuning Range: This is the range of frequencies possible for tune, also clarified on fig. 5.1. The choice of the tuning range of a VCO is an important parameter and can be specified using two main parameters [14]:

1. The effect of temperature and random process variations on the center frequency of the oscillator.

2. The frequency range required for operation, that is, for frequency modulation or for switching between frequency bands in some cases as well.

Temperature and process variations should be seriously taken into account; changes in frequency up to twice the center frequency can occur based on such random processes [5]. It is thus safe to sometimes try and aim for the highest possible tuning range within the power and area constraints posed by the design.

Although what has just been said strongly implies that the K_{VCO} should be as large as possible to achieve a large tuning range, this can also bring disadvantages. Noise on the tuning input lines is inevitable and if the tuning sensitivity is of a large enough value, the frequency could be greatly varied, which is an undesired effect. It can also be seen from eqn. 5.1 that any noise affecting K_{VCO} will directly and proportionally affect the output frequency. Not only does a large K_{VCO} degrade phase noise due to its large frequency variation but also consumes much power to start up oscillation [15].

One method to overcome the predicament presented (that K_{VCO} should be as large and as small as possible at the same time) is to divide a large frequency range into sub-bands, this is done in this work, in the crossed coupled oscillators by introducing discrete digital tune alongside the analog tune, effectively decreasing the tuning sensitivity to half. This is discussed in detail in this and the following chapters.

Tuning Linearity: As shown in fig. 5.1 the tuning sensitivity is seldom constant, and shows nonlinearities; K_{VCO} is usually low at the two extremes and high in the center region, higher than the expected value. Poor tuning linearity is not desired for VCOs because it degrades the settling behavior of phase locked loops [5]. It is thus important to have the K_{VCO} as close as possible to being constant for the chosen frequency range.

Output Voltage Swing: A large output swing makes the oscillator output signal less prone to noise. A large output swing however demands greater power consumption and larger supply voltage and will reduce the tuning range as well

(This is discussed in more detail in section 5.2).

Power Consumption: An important factor which is involved in many trade-offs between output swing, tuning range, spectral purity, area, speed and noise. To improve any area of an oscillator it is usually the case that the consumed power increases.

Frequency pushing and Noise immunity: Sensitivity to supply voltage is called "frequency pushing". Noise is a general problem in oscillators, as discussed, at the tuning inputs and also on the supply rail. It is critical (but difficult) to design the oscillator for high noise immunity. Differential implementations have the advantage of suppressing most common-mode noise in any signal, an advantage not present in single-ended implementations. It is therefore best to design differential paths for the local oscillator (LO) signal as well as differential tuning inputs when possible.

Output Signal Purity: Noise causes unwanted distortion in the output signals, it is impossible to have a perfectly pure sinusoidal output due to *electronic noise* present in the used devices. Unwanted variations in frequency (jitter) and phase (phase noise) are the two unwanted results of such noise, these two quantities should be reduced as much as possible when good spectral purity is required.

5.2   Frequency Tune in LC Oscillators

It was proved before that the oscillating frequency of an LC oscillator is a function of both inductance and capacitance ($f = \frac{1}{2\pi\sqrt{LC}}$), therefore tune in such oscillators can be done by changing the values of the capacitors and inductors. In general, it is the capacitor tank that is used for tuning since it is easier to manipulate and create in a variable form as a varactor. Not to mention that capacitors have better quality factors and smaller area as well when compared to inductors therefore using more than one of them is usually the better choice. Tuning methods can be divided into two branches, discrete frequency tune or continuous frequency tune. This is discussed now in detail.

5.2.1   Continuous Frequency Tune

Continuous change in frequency indicates the use of a component in which the capacitance can be continuously varied using a control input such as voltage or current. Such a component exists, it is called a varactor, and is discussed in

detail in chapter 3.
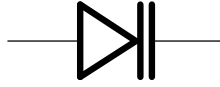
Figure 5.2: Schematic symbol of a varactor.

A varactor can replace the capacitor in any LC oscillator circuit thus providing tune of the capacitance value and therefore the frequency as well. Varactors, however, show a non-linear change of capacitance with voltage, imposing constraints on the used frequency range.
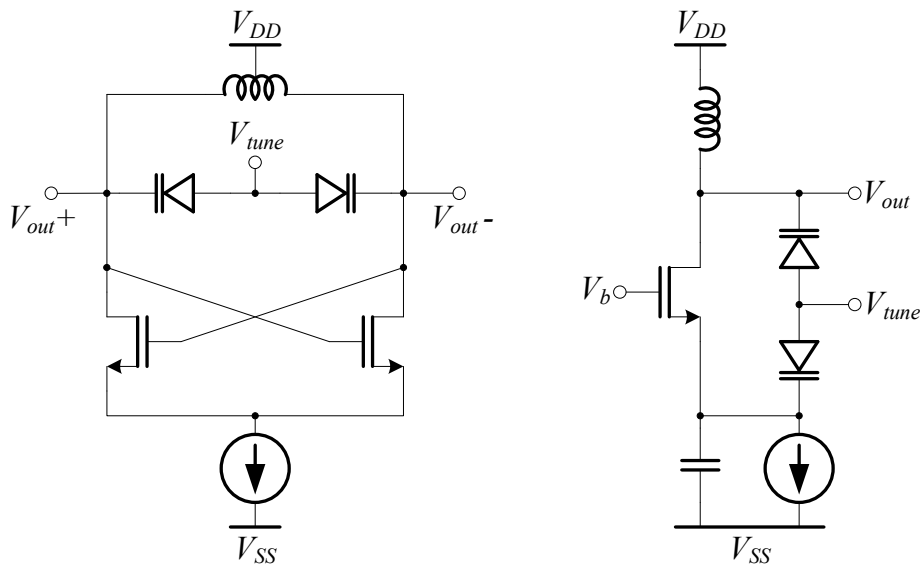
Figure 5.3: Capacitors replaced by varactors in a) cross-coupled and b) colpitts oscillators.

Operation of the varactor depend on the capacitance due to reverse biasing a diode, this therefore imposes limits on the tuning voltage range. To clarify, consider fig. 5.4, this shows the output swing of the cross-coupled oscillator in fig. 5.3, the potential difference across the varactor diodes must always be negative (or positive but lower than V_{th}) for correct operation of a variable capacitor. The allowable range of V_{tune} is therefore as marked on fig. 5.4; it is clear that this range forces the diode always to be reverse biased, by placing the constraint that the difference between V_{tune} and $V_{out}+$ (or $V_{out}-$) will always be lower than the diode's threshold voltage (V_{th}). If the amplitude of the LO waveform is A then

the range of V_{tune} can be expressed as follows.

$$V_{SS} < V_{tune} < (V_{DD} - A + V_{th}) \tag{5.2}$$

Tuning range therefore *trades-off* with output voltage swing, this was mentioned before, and is clear here from the above explanation and fig. 5.4. From this figure it can also be seen that the capacitance cannot be constant, since the tuning voltage varies with the oscillating voltage, however it is an *effective* average capacitance that is still a function of V_{tune}.
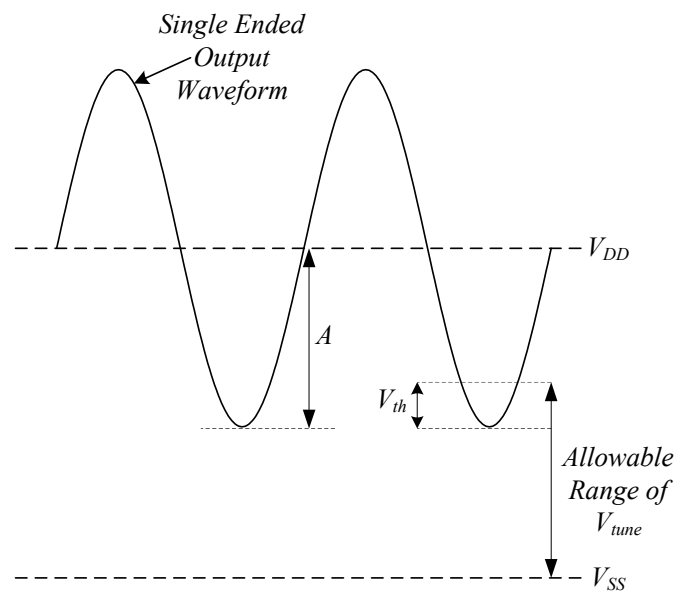
Figure 5.4: Allowable range of the varactor tune voltage.

5.2.2 Discrete Frequency Tune

It is tricky to achieve a wide tuning range, which also means a high K_{VCO} value, while maintaining low phase noise, power consumption and input noise sensitivity [15]. There is usually a trade-off between these values preventing further improvements. One way to avoid this is to split the tuning range into smaller frequency sub-ranges by using discrete digital tuning methods presented here. It also decreases the K_{VCO} by at least half therefore improving many areas of the oscillator while maintaining a higher tuning range.

For discrete frequency tune it is also the case that the capacitors are best to be used, as mentioned before, because of their better quality factors and more compact areas. The basic block used for digital tune would be using a capacitor

and a switch, this is shown in fig. 5.5 with two switches to achieve symmetry in the structure.
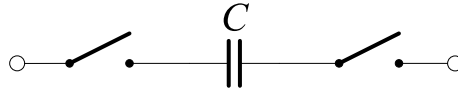
Figure 5.5: A digitally switched capacitor.

The structure of the switched capacitor (shown in fig. 5.5) allows the discrete change of frequency by adding or removing capacitance controlled by the switches. It is therefore made possible to create discrete changes of frequency with different switch combinations. The structure can have capacitors of any arbitrary values but it is best to have a binary weighted array in which capacitors start from $2^0 \times C$ then $2^1 \times C$, $2^2 \times C$, and so on, following the pattern of $2^{n-1} \times C$, where n is a natural number starting from 1. The reason behind having a binary weighted array is to achieve a constant increase of capacitance with each increment in switching, which will also translate into a uniform change in frequency.

To elaborate, consider a 2-bit binary weighted capacitor bank (refer to fig. 5.6), the possible values for V_0 and V_1 are 00, 01, 10 and 11, by observation it can be seen that the value for equivalent capacitance (of the digitally switched section only) is 0, C, 2C and 3C respectively, hence a uniform change in capacitance which will translate into a uniform variation in frequency as well.

Figure 5.7 shows the output tuning characteristic that would result from such a band-switched capacitor bank of size two. The four resulting curves are due to the possible combinations of turning-on or off two switches ($2^2 = 4$). It is obvious that the uppermost curve (Band 1) occurs when no switch is turned on; the highest frequencies correspond to the lowest capacitance. At each frequency band the frequency can be continuously tuned using analog tune provided by the varactor.

It is worthy to note how the tuning sensitivity (or the slope of the tuning curve) decreases with increasing the frequency band, this effect is simply due to the fact that when more capacitance is added, the variable capacitance change (ΔC_{var}) of the varactor becomes a smaller fraction of the total, thus smaller analog tune is observed for lower frequencies.

It is instructive to now take a look at the equations [15] that would govern the design of such a band switched capacitor array, taking fig. 5.6 for reference. The following equations can be derived for the equivalent frequency at each band.
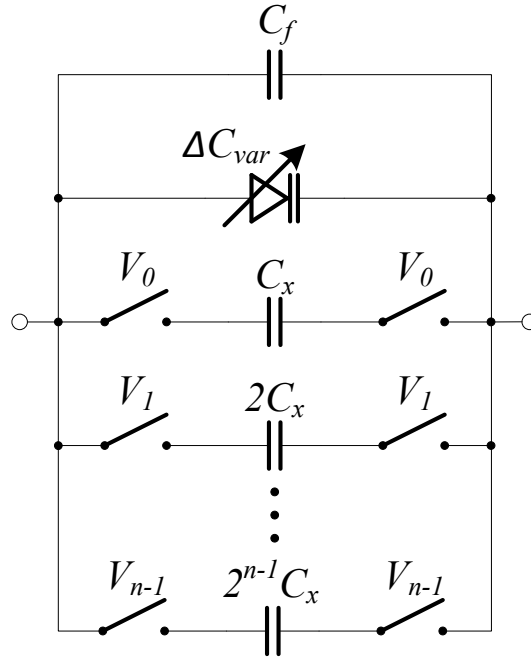
Figure 5.6: Arrangement of a binary weighted capacitor bank.

"n" here is the size of the capacitor array.

$$f_{osc}(band1) = \frac{1}{2\pi\sqrt{L(C_f + \Delta C_{var} + (2^n - 4)C_x)}} \tag{5.3}$$

$$f_{osc}(band2) = \frac{1}{2\pi\sqrt{L(C_f + \Delta C_{var} + (2^n - 3)C_x)}} \tag{5.4}$$

$$f_{osc}(band3) = \frac{1}{2\pi\sqrt{L(C_f + \Delta C_{var} + (2^n - 2)C_x)}} \tag{5.5}$$

$$f_{osc}(band4) = \frac{1}{2\pi\sqrt{L(C_f + \Delta C_{var} + (2^n - 1)C_x)}} \tag{5.6}$$

An important parameter which is widely discussed in [15] can be extracted from the the plot in fig. 5.7. It is the overlap (ov) of the frequency bands, it is usually chosen to be $\frac{1}{2}$ [15], in order to cover each frequency by at least two frequency bands.

It was mentioned earlier that K_{VCO} decreases when we switch-on more capacitors, this can be proven numerically. K_{VCO} for each sub-band would be defined as the ratio of frequency range in that sub-band to that of band 1. For simplicity,
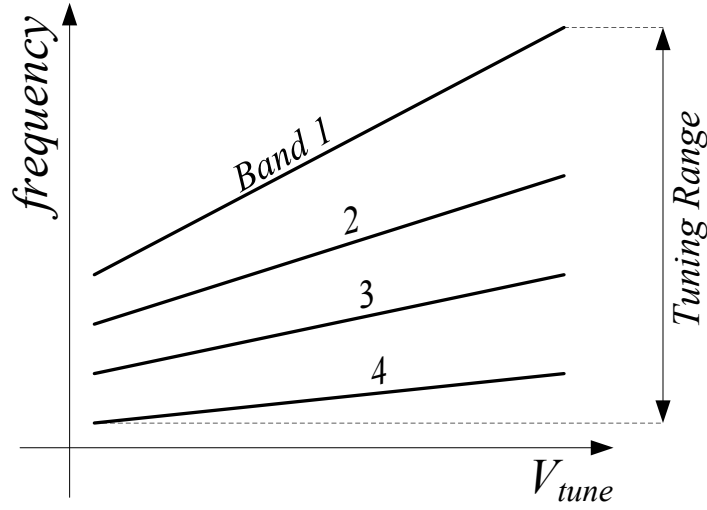
Figure 5.7: Tuning characteristic of a 2-bit capacitor array.

$C_f = 0$, and $ov = \frac{1}{2}$ which leads to choosing C_x to be half of ΔC_{var}, the K_{VCO} is obtained as the frequency range at each band divided by that at band 1. [15].

$$K_1 = \frac{\sqrt{\Delta C_{var}}}{\sqrt{\Delta C_{var}}} = 1 \tag{5.7}$$

$$K_2 = \frac{\sqrt{\Delta C_{var}}}{\sqrt{C_x + \Delta C_{var}}} = \frac{\sqrt{1}}{\sqrt{0.5 + 1}} = 0.816 \tag{5.8}$$

$$K_3 = \frac{\sqrt{\Delta C_{var}}}{\sqrt{2C_x + \Delta C_{var}}} = \frac{\sqrt{1}}{\sqrt{1 + 1}} = 0.707 \tag{5.9}$$

$$K_4 = \frac{\sqrt{\Delta C_{var}}}{\sqrt{3C_x + \Delta C_{var}}} = \frac{\sqrt{1}}{\sqrt{1.5 + 1}} = 0.632 \tag{5.10}$$

From the above, the overall tuning range (TR) of the capacitor tank can be obtained [15] as a function of the band overlap (ov), the oscillating frequency at the highest band ($f_{osc}(band1)$) and tuning sensitivity (K_i) [15].

$$TR = (1 - ov)[f_{osc}(band1)][\sum_{i=1}^{n^2-1} K_i + \frac{K_{n^2}}{1 - ov}] \tag{5.11}$$

5.3   Frequency Tune in Ring Oscillators

Since Ring oscillators have a theory of operation different to LC oscillators, they also have tuning methods which are different and specific to them. These are

briefly discussed and compared here.

5.3.1 Load Control

The first intuitive method in varying frequency of oscillation is to change the time constant (τ) of an inverter. The time constant depends on two variables: the capacitance and resistance presented in the circuit, therefore those are the two degrees of freedom provided. The capacitance at the output can be intentionally placed or parasitic, either way, control of the capacitor can be done by replacing a fixed capacitor by a varactor. This is however impractical since it consumes large area unnecessarily. The other variable that affects τ, the resistance, can be varied as shown in fig. 5.8 simply by controlling the effective resistance in the CML stage, done through varying the gate voltage of the load transistors.
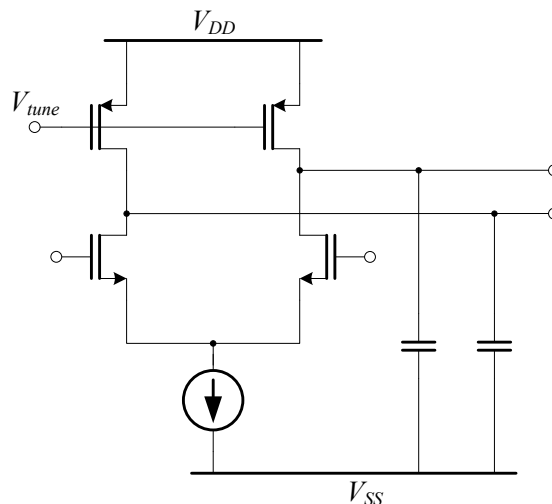
Figure 5.8: CML inverter with variable load.

The problem with this tuning method is that the amplitude varies with frequency, which is undesired. There are methods [5] which could be done to overcome this by compensating the amplitude variation with additional current control, but the circuitry is bulky since it requires an additional amplifier.

5.3.2 Current Steering

The method of tune which is found most simple to implement, yet effective as well, is to vary the tail current in all the inverter stages. This tuning method has the advantage of a very wide tuning range; it can change the frequency from DC up to whichever frequency the ring oscillator can support, up to four orders

of magnitude of frequency tune [5]. The disadvantage presented by this method is that the amplitude varies greatly, in orders of magnitude [5] when the current is varied as mentioned in a CML inverter for example. This is however avoidable as shown in fig. 5.9 by adding a PMOS pull-up transistor in parallel with the load, which compensates for the amplitude drop with current. Another solution as well [16] is simply to not use the CML-based ring oscillator, rather a CMOS-inverter-based oscillator, which can be thought of as the CML stage in part b) of fig. 5.9 with the load removed completely. This causes the amplitude to remain constant, or almost constant, across different values of frequency tune.
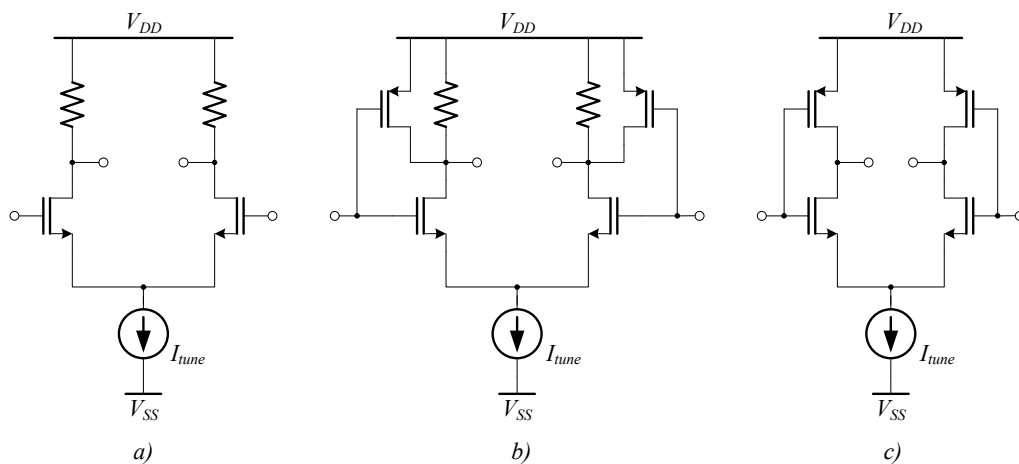
Figure 5.9: Differential ring oscillator stages: a) CML inverter, b) CML inverter with pull-up transistor, c) CMOS inverter.

5.3.3 Interpolation

"Interpolation" [17] is yet another method that could be used to create a tunable ring oscillator. It is based on creating two paths for the signal, a fast and slow path. These two paths are then summed at the output and the total signal at the output is the mixture of both. The amplitude of each of the slow and fast paths is controlled; effectively varying the frequency from that of the slow path to that of the fast one by having opposite control at the slow and fast paths.

The disadvantages here are obvious: since two ring oscillators need to be constructed, the area is immediately multiplied by two, not to mention the summation stage at the output as well. The circuit also has a greater degree of complexity.
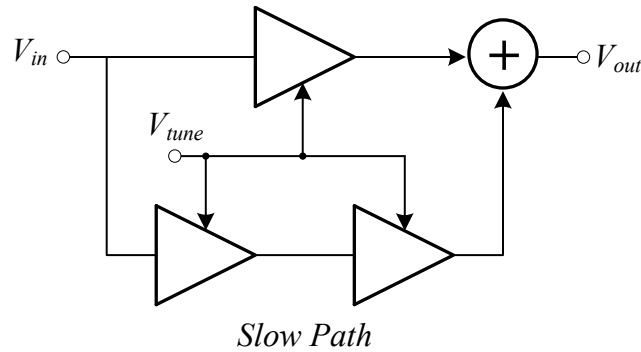
Figure 5.10: Delay variation by interpolation.

5.3.4   Positive Feedback

This tuning method can be better understood after understanding "load control" in section 5.3.1. It relies on the same principle being the variation of the load in the inverter to arrive at a different frequency. The method used here however uses the phenomenon of *negative resistance* which is discussed when talking about cross-coupled oscillator (chap. 4).

The *negative resistance* used here is a cross-coupled transistor pair as well, which is proven to provide $R = \frac{-2}{g_m}$. It can be placed in parallel with the load as shown in fig. 5.11 to vary the value of the load resistance hence the time constant as well and the frequency. Consider the half circuit in fig. 5.11, the equivalent resistance would be the parallel combination:

$$R_{eq} = R_p \parallel (-\frac{1}{g_m}) = \frac{R_p}{1 - g_m R_p} \tag{5.12}$$

and the transconductance is controlled by the bias current of the cross-coupled pair, the greater the current, the greater g_m becomes and therefore the resistance will be less negative.

This tuning method does not provide a large tuning range, approximately two-to-one [5]. It also suffers from the problem faced by most other mentioned ones: The amplitude still varies with tune. To reduce this problem I_{SS} can be varied opposite to I_{tune} thereby keeping the total current between the 2 sources a constant [5]. To further explain, consider fig. 5.12, the frequency tune controls are now applied in differential form and they will simultaneously reduce the current in one branch while increasing the other. This will assure that a constant current is applied in total and avoid the problem of amplitude variation with frequency. In one half-cycle, current will reach the resistor R_1 through both M_1 and M_3, and in the other half-cycle, the same will happen for R_2, through M_2 and M_4, therefore a total (and constant) swing equal to $2R_p I_T$ will be the result.
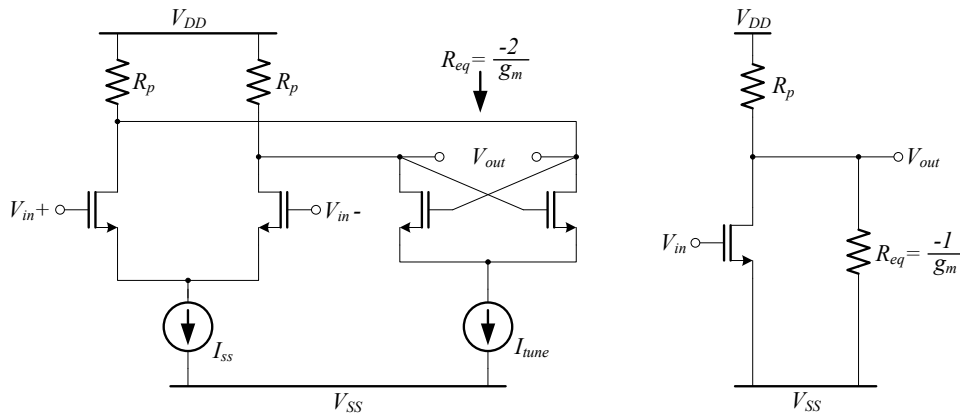
Figure 5.11: CML inverter with negative resistance load.

Another advantage is having a differential tuning input, which increases the noise immunity of the oscillator.

It can be immediately observed however that this remedy has a big disadvantage; it consumes more voltage headroom since there will effectively be 2 transistors, a resistor and a current source in the path from V_{DD} to V_{SS}. This will provide tighter constraints to keep the differential pair transistors in saturation mode [5]. It is therefore apparent that there exists a trade-off between voltage headroom and sensitivity of the output amplitude. In applications where low supply voltages are used, this topology might not be the best choice, but this is also avoidable by using current folding topology for the current inputs [5].

A couple more notes that should be mentioned about the used topology is that the current in the I_{SS} branch must not drop to zero in order to allow for correct biasing in the CML stage, for correct operation of the circuitry. It has also been reported [5] that this method provides reasonable tuning linearity. Furthermore, the circuit requires careful simulations to assure correct transistor operation modes across all tuning ranges of interest, it is tricky to fulfill all the conditions all the time.
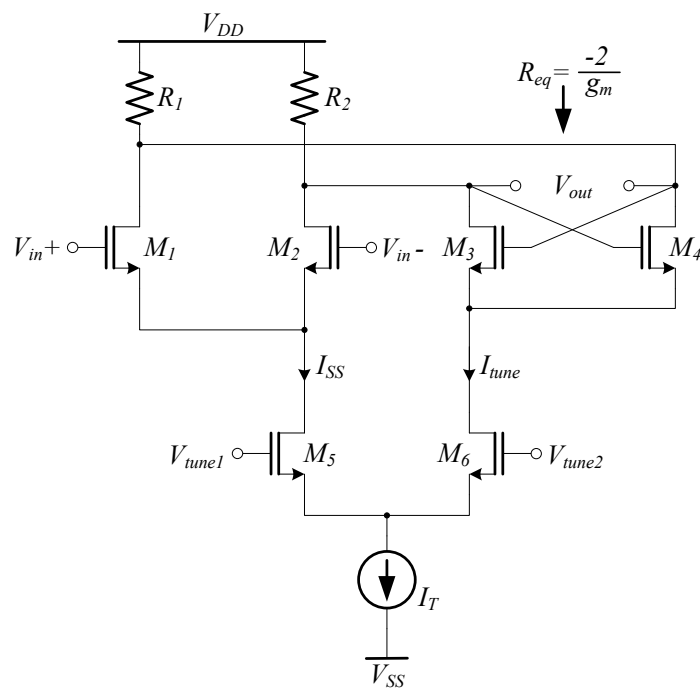
Figure 5.12: Current steering applied to avoid amplitude variation with frequency.

Chapter 6

Transmitter Design

The theory that goes into designing a transmitter with its various components has been discussed in the previous chapters. The design started by doing the modeling and measurements of components in the new Gateforest® technology used, then the application of the measurement data for model construction used in simulations of the circuits.

This chapter utilizes the gained knowledge from the theory of operation, and the various design equations proven to be able to put together the various sub-circuits that are required for the full transmitter circuit. The design procedures and methodology are already discussed in the previous sections so this chapter merely indicates the design choices and why each of them is made. Design values are provided in appendix A.

The designed transmitter topologies are chosen to have direct modulation inputs which eliminates the need for mixers or filters in the design, this is done to reduce the complexity of the circuit which is important since a new technology is being tested.

It is instructive to start this chapter with an overview of the modulation methods used. Frequency shift keying (FSK) and Amplitude shift keying (ASK) modulation methods are used in the transmitters. They are both types of digital modulation, for FSK modulation the digital "0" and digital "1" are each assigned a different frequency at a small offset from the other. In the case of amplitude modulation each digital value is assigned a different amplitude value. This is clarified in fig. 6.1.

6.1 Cross-Coupled VCOs

Cross-coupled oscillators are LC oscillators that are implemented here for two frequencies: 869 MHz SRD band and 2.45 GHz ISM band.
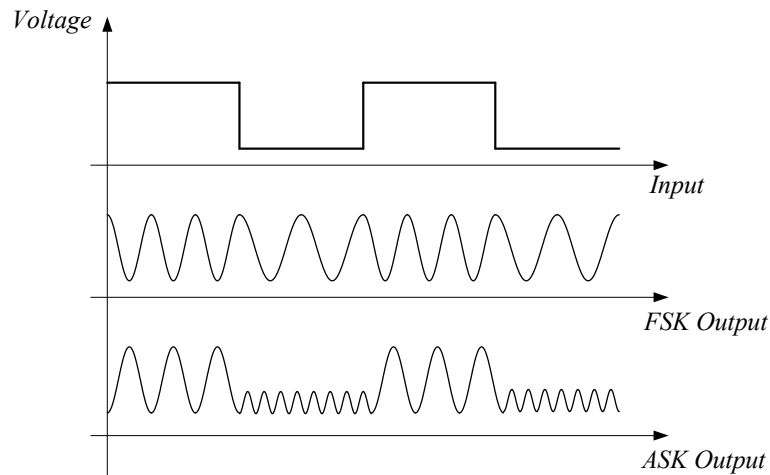
Figure 6.1: FSK and ASK modulation.

6.1.1   Circuit Topology and Biasing

The basic structure for cross-coupled oscillators consist of at least n-channel cross-coupled transistors. As discussed in chapter 4 this provides the so-called *negative resistance* which is essential for operation of an LC oscillator. For this design, simulations are run for two circuits: one with both NMOS and PMOS cross-coupling, and the other only with an NMOS cross-coupled pair. Both designs are compared in terms of area and power consumption and the design with both types (NMOS and PMOS) cross-coupling is found to be the more efficient and is therefore chosen for circuit design.

Although omitting the current source improves phase noise [14] as well as voltage headroom, it is still used here because phase noise is not an important issue of discussion when investigating the new technology. The difference of 5V between the two supplies is also sufficient and no headroom problems occurred. Furthermore, the use of a current source makes the design more robust for a large voltage swing since it makes the biasing of the transistors less sensitive to oscillation voltages.

The current source is designed as a simple current generation branch and mirror as shown in fig. 6.2. The current source is constructed from transistors M_{n3} and M_{n5} while the mirror is transistor M_{n4}. The minimum transistor size is chosen for M_{n3} and the other transistors are sized appropriately to achieve the required current. This method ensured smallest area.
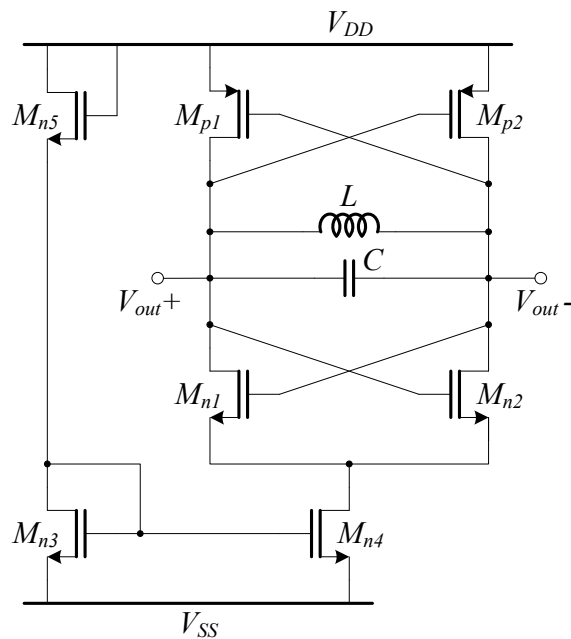
Figure 6.2: A simple cross-coupled complementary oscillator.

6.1.2 Analog Frequency Tune and Modulation

Analog frequency tune could only be done through continuous tune of a component that controls the frequency, these are proved to be the inductor and capacitor in chapter 5. It is also earlier discussed that variable inductors do not exist, therefore varactors (see section 3.1) are used for that purpose. It is shown that varactors have a capacitance which is dependent on the voltage applied across it. Large varactors are used to achieve a wide tuning range.
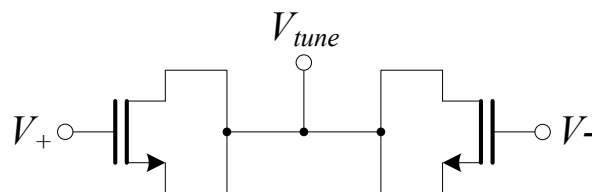
Figure 6.3: Differential varactor implementation.

To have a differential varactor, the sub-circuit in fig. 6.3 is implemented [18]. In the same figure also note that the gate terminals of the varactors are chosen to be the ones connected to the oscillation nodes. This is done in order to decrease the parasitic capacitance added to oscillation nodes due to the varactor, which are expected and calculated to be larger from the source and drain terminals

than from the gate. Although a PMOS implementation would have resulted in a wider tuning range, the NMOS alternative is chosen since it has a more reasonable range of tuning voltages.
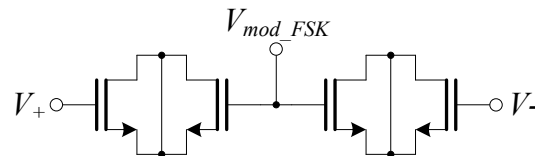
Figure 6.4: Differential modulation varactor.

Frequency modulation could be done through the tuning varactor by pulling the LO signal frequency, but to do that and have a small frequency offset would be difficult and error-prone. It would also be difficult to control due to the large varactor's non-linearity [19]. This problem is circumvented by using a separate small varactor dedicated only for modulation input. This is shown in fig. 6.4 and it can be seen that two varactors are placed back-to-back to reduce the effective capacitance as much as possible. This is to arrive at the required small frequency offset.

6.1.3 Digital Frequency Tune

Digital tune in the case of the designed VCO implies the discrete increase/decrease of frequency controlled by a series of switches. As mentioned before, frequency in LC oscillators is a function of capacitance and inductance present in the circuit. It is therefore intuitive that digital tune can be done by adding or removing capacitors or inductors from the oscillator circuit. Capacitors are chosen for this.

Switch Design

In designing the electronic switches to control turning-on and off capacitance, the capacitors' efficiency, power consumption and parasitic resistance had to be taken into account. The first two parameters are to be optimized while the third variable is to be minimized as much as possible. Fig. 6.5 shows how the switch design developed: starting with the switch in (a).

It is first thought of to have regular pass-gate logic in which two transistors control whether the branch is added or not, transmission gates comprising of both NMOS and PMOS transistors are also investigated. This method however generally shows poor performance in that the switches are required to be quite large and added a lot of parasitic resistance to the oscillation nodes which in turn increased power consumption and deteriorated VCO performance.

An alternative [15] had to be thought of in which parasitic losses in the switches are minimized, this is shown in part (b) of fig. 6.5. This requires more capacitors but is better because the capacitors have high quality factors. A modification is done to this as well to maximize its switching capacitance: the third capacitor in the middle is removed completely as shown in part (c) of the same figure.
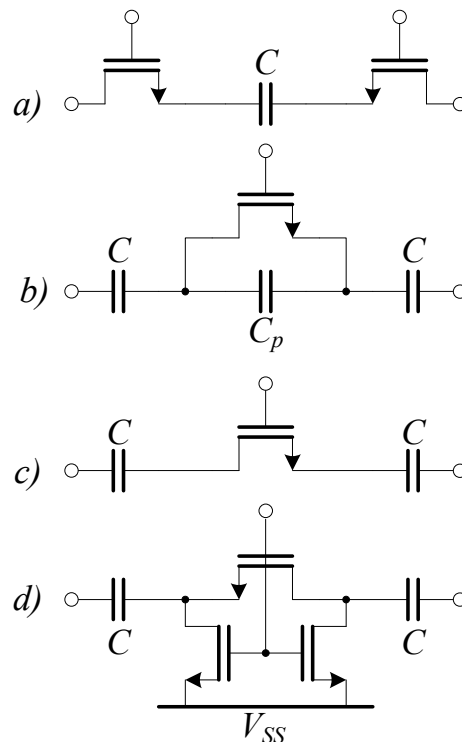
Figure 6.5: Switch design development.

The switch in fig. 6.5(c) simulated very well; it has acceptable parasitic losses and had good switching characteristics. The problem with it however is that it has the source and drain as floating nodes, which is something that does not affect simulation but will affect the actual circuit. Here is why: the simulation tool used treats any floating nodes as grounds during simulation run, this is however not true in the actual case because they could have any voltage on them according to stored charges or any external factor. This is not acceptable because in that case the behavior could be unpredictable.

To overcome the problem just discussed, 2 transistors are added to the switch as shown in part (d) of fig. 6.5 which ensures that those two nodes (at the source and drain of the transistor) will be pulled to ground once the transistor is on, providing it with a predictable behavior and correct operation.

One last consideration in designing the switches is their sizes, according to the following equation:

$$I = C\frac{dV}{dt} \tag{6.1}$$

it is shown that a larger capacitor would require a higher current, hence a larger switch as well, so the switches are sized accordingly.

Capacitor Bank Sizing

When designing the the capacitor sizes to achieve tune for a specific frequency range ideal capacitors are first assumed and the design equations presented in section 5.2.2 should be used for first design. As mentioned in that same section, a binary-weighted capacitor bank is used such that each increment of digital tune value (ie. the change from 00 01 10 to 11) would result in a homogeneous increase in capacitance leading to a uniform shift of frequency.
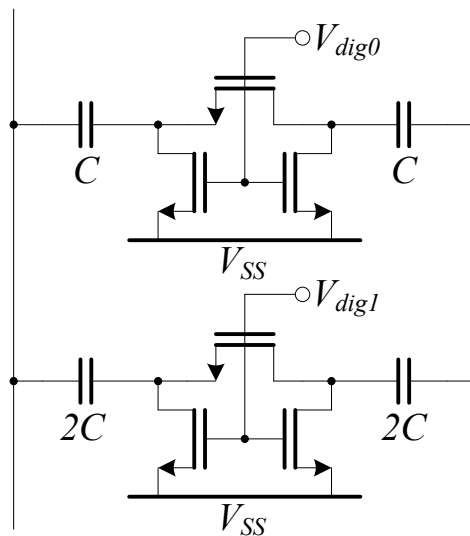
Figure 6.6: The designed 2-bit digitally-controlled capacitor bank.

As it is the case in [15] the design using equations is never accurate since it presents the ideal case. For that, a simulation tool is required to accurately simulate the structure. Simulations are applied on the capacitor bank structure and optimized to arrive at the output characteristics required, after fabrication and measurements there is still more deviation expected in the frequency tuning plots. Another note worthy of mentioning is that the LO amplitude drops when

more switches are operating, the reason for this is the increase in number of operating switches which introduce losses as well to the system.

The VCO designed is going to be part of a wireless RFID system therefore will not have any physical controls or switches. For that reason, and according to application it may be required to use serial input of the digital tune binary values. In this case, a suggestion for future work is to have a serial-to-parallel converter as well as latches at the digital-tune inputs to store the tune values, so that a serial binary value could be used.

6.1.4 Complete VCO

The entire VCO is now brought together simply by appending the various tuning-capacitor components in parallel to form a capacitor bank with a certain equivalent capacitance that has a changeable value according to inputs. The cross-coupled VCO is still in principle a lossy resonator with an active circuit component (the cross-coupled transistors) to compensate for that loss and sustain oscillation. Fig. 6.7 shows the entire oscillator and clarifies the discussed sub-circuits.

6.1.5 Output Stage

The output stage of the transmitter serves three purposes:

1. To isolate the VCO from the load thereby avoiding or minimizing frequency pulling.

2. To have a 50Ω driving capability, that is, to be able to provide enough output current and maintain an acceptable voltage swing.

3. To have amplitude control for optional ASK modulation.

The reason that the output had to drive a 50Ω load, is so that it can be used with the measurement probes (which are 50Ω matched) and the measurement equipment (which have 50Ω load termination). If the transmitter is to be used in an actual RFID, not one that is meant for measurement, the redesign of the output stage is necessary to conform to the new requirements. That would probably be an antenna termination.

From fig. 6.8 the three stages in the output amplifier can be distinguished. The first one is a buffer, with small transistors used in the differential pair to load the oscillator as little as possible. The CML buffer is followed by another one which has a variable tail current. By varying the value of this current, the amplitude of the output signal is also changed and is therefore used in ASK
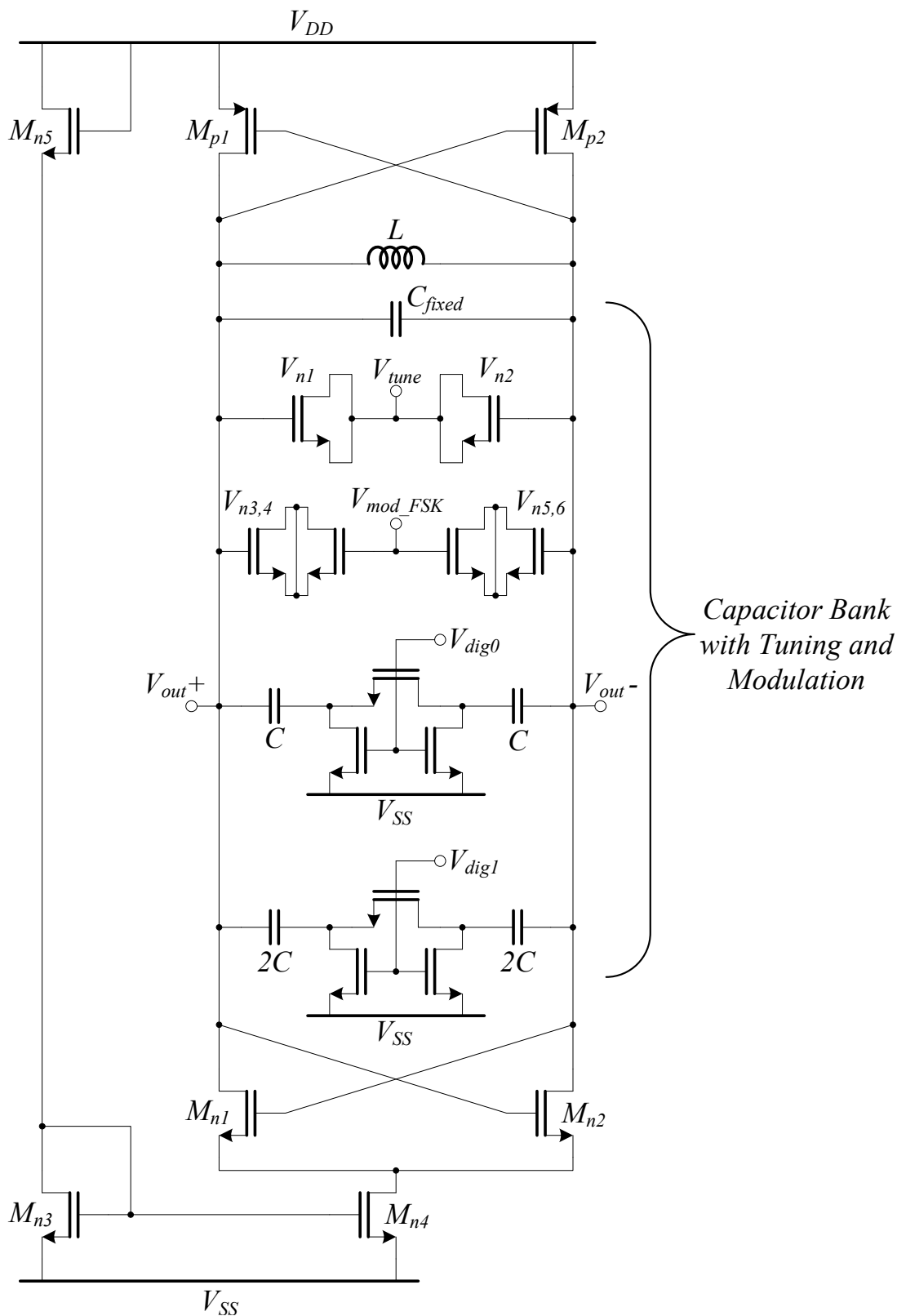
Figure 6.7: Schematic of the proposed cross-coupled VCO.
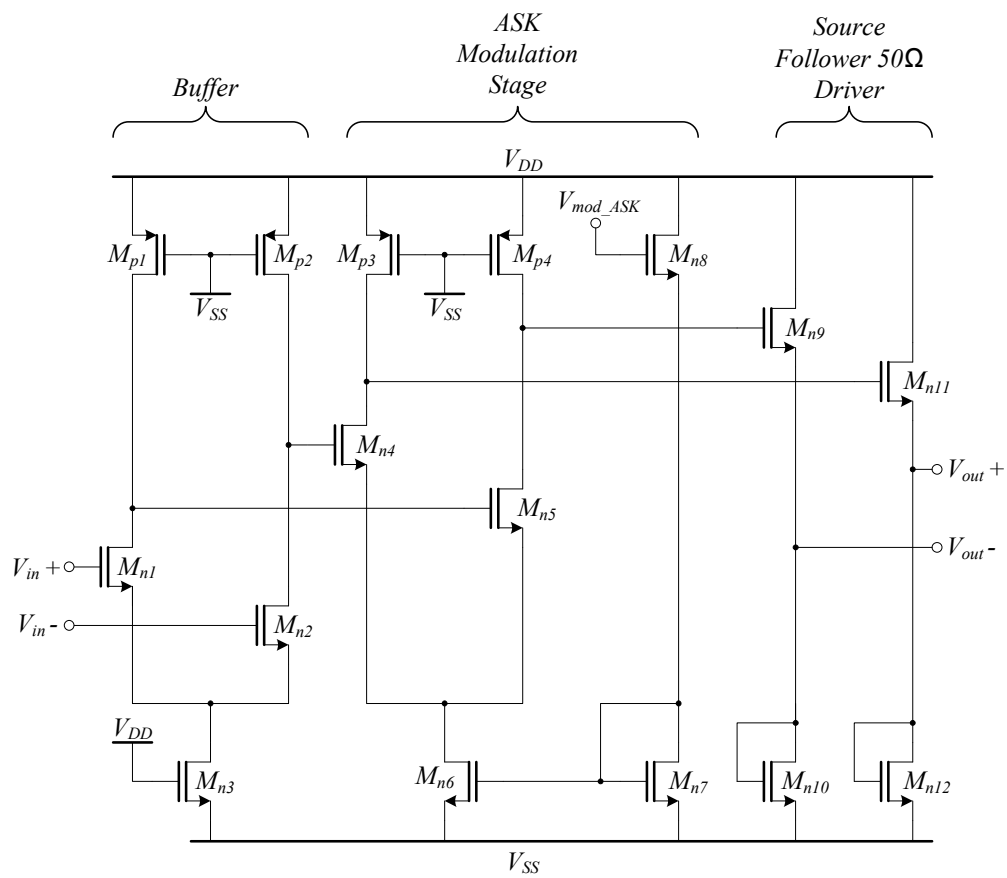
Figure 6.8: Schematic of the proposed output stage.

modulation. The final stage comprises of two source followers, one at each of the differential outputs. The transistors used in these drivers are large so that they can provide enough current for the 50Ω termination.

6.2   Differential Ring Oscillator

The design of a ring oscillator is always simple, as shown in fig. 6.9, it consists basically of a chain of inverters in a feedback loop. The design concepts behind it are discussed in chapter 4.
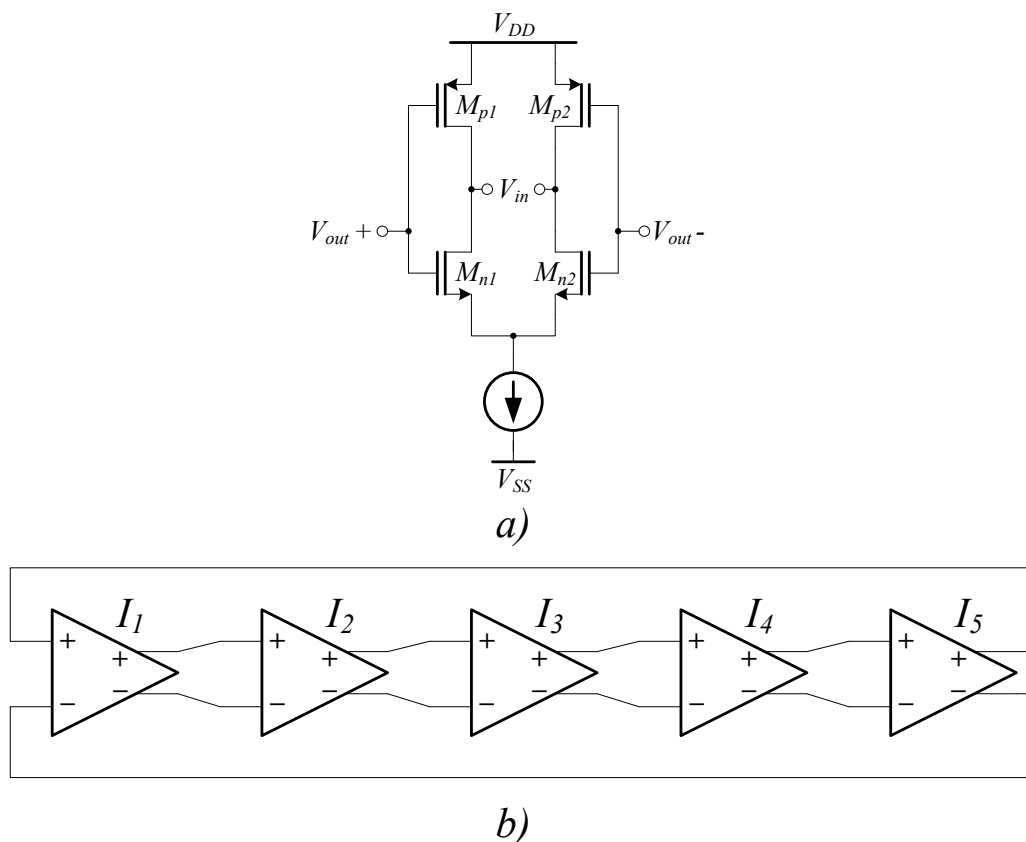
Figure 6.9: a) One CMOS inverter. b) Block diagram of ring oscillator.

A differential CMOS ring oscillator is designed with power consumption and area in mind, for that, the minimum transistor size, that is, one finger is used in each of the transistors used in the inverters. No intermediate capacitors are used between the stages as well since they are found unnecessary, this also widens the frequency range in which the oscillator could be used.

Note that since this VCO has a differential topology, therefore the same

output stage is used as with the cross-coupled oscillator (see section 6.1.5). The modulation type is amplitude modulation and is done at the output stage as clarified earlier.

Analog Frequency Tune

The frequency of a ring oscillator can be tuned through the control of the tail current of the inverters. In this case the frequency increases with current and on the other end, it can be reduced theoretically until DC frequency. In CML-based ring oscillators, this tune method usually presents the problem of amplitude variation with tune current, this is however not the case for the topology chosen here; CMOS configuration assures the full amplitude swing of the signal due to the PMOS pull-up transistor.
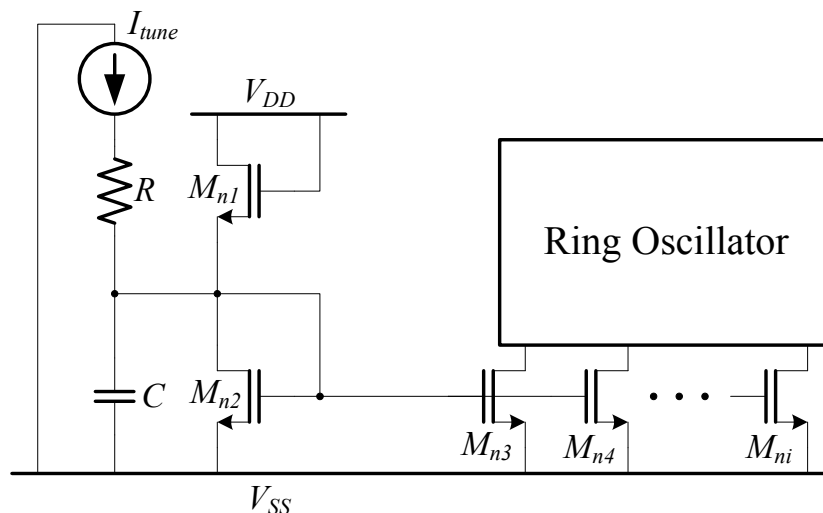
Figure 6.10: Current steering circuit for ring oscillators.

Current steering is done though injecting or sourcing current from the current generation branch in a simple current bias circuit. This biasing current is then also copied using a current mirror to each of the inverters as well with the copying transistors sized such that they can provide the maximum current required.

6.3 Single-Ended Ring Oscillator

The single-ended ring oscillator is designed very similarly to the differential one. It consists of seven CMOS inverter stages with minimum sizes for each inverter, there are also no intermediate capacitors between the stages. Biasing for this

ring oscillator as well as analog tune (through current steering) is done using the same circuit used for the differential implementation discussed in section 6.2.
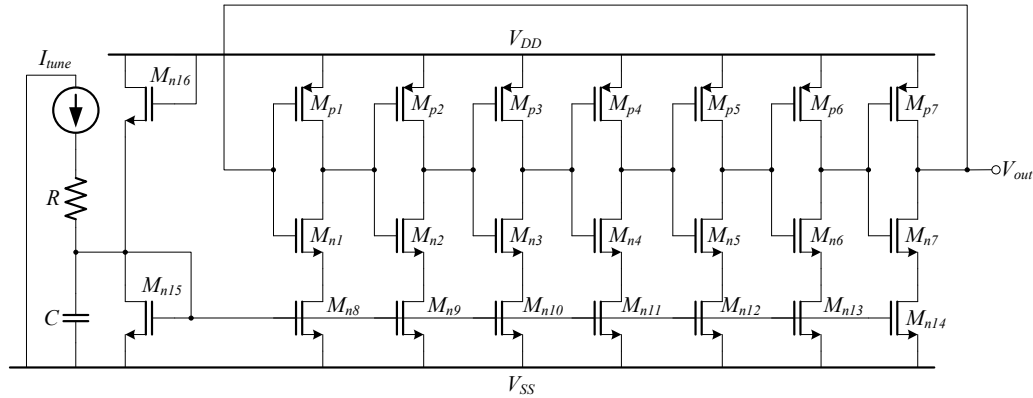
Figure 6.11: Single-ended ring oscillator schematic.

This tuning method is chosen because it results in a wide tuning range and has low complexity and little area consumption.

Output Stage

This is a CMOS output stage which when compared to the previous CML-based output stage, it is expected to have lower power consumption because there is no static power dissipation in a CMOS inverter [12]. The implementation is simple and designed again to fulfill the same three requirements listed in section 6.1.5.

The Output stage consists of 3 blocks and are marked on fig. 6.12. It is composed simply of two CMOS inverters one after the other and a pull-to-ground NMOS transistor for amplitude control. The first inverter is a buffer with very small transistors to buffer the oscillation output and minimize any effects of frequency pulling by the load. The used transistor size here is small so as not to add much parasitic capacitance to the oscillation nodes.

Following the buffer is another CMOS inverter which has the purpose of driving the 50Ω load. It therefore has large transistor sizes in order to be able to output enough current while maintaining a voltage swing large enough to be read on the measurement equipment that are to be connected.

The final stage is an amplitude control unit composed of a single transistor. This is the simplest way to have amplitude modulation input in such an output stage. When a positive voltage is placed on the gate of this transistor, it will switch on and pull the signal to ground. The strength of pulling is balanced by the PMOS transistor in the CMOS inverter before it and therefore a suitable input voltage for ASK modulation can be calibrated to have the ratio required for the digital "1" and "0".
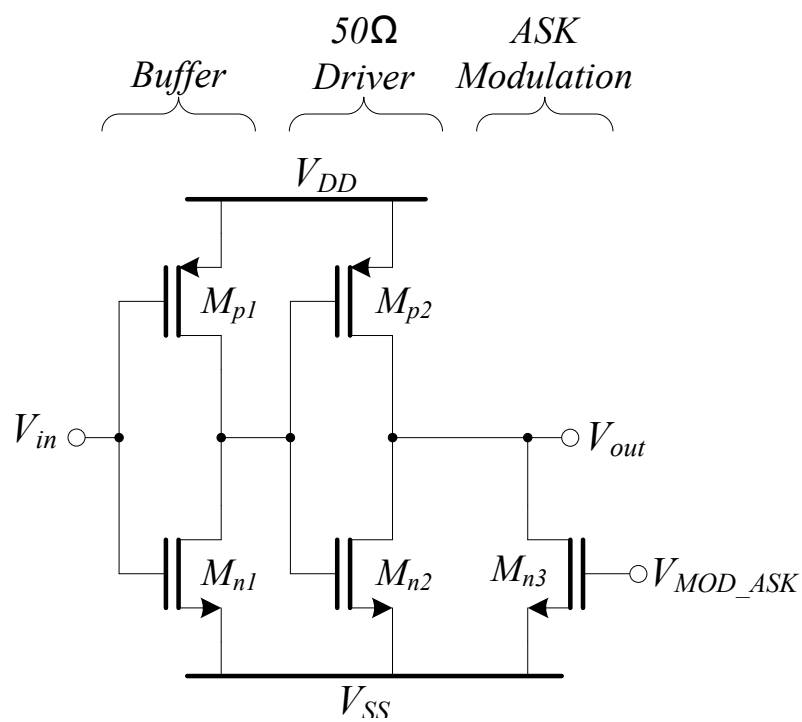
Figure 6.12: Proposed output stage for the single-ended ring VCO.

Chapter 7

Simulation Results

In this section, the simulation results of the designed transmitters are presented. The used simulator has more than one option for simulating oscillator circuits, the first and obvious option is a transient simulation, the second is to run a Harmonic Balance (HB) or Circuit Envelope(CE) simulation with the oscillator function chosen and the oscillating nodes specified.

The second mentioned simulation alternative is easier to use and more useful due to the built in functions that would output plots such as phase-noise or harmonic components at no extra effort. It does however suffer one major setback: the solvers used are not robust enough and occasionally failed to converge. This is usually not the case for oscillators that output a pure sinusoid, such as the cross coupled oscillators, but for the ring oscillators, there is a lot of distortion in the output signals making it difficult to simulate using HB or CE. Transient simulations were run for these circuits instead.

7.1 Cross-coupled Oscillators

Cross coupled oscillators generally show higher spectral purity in the output waveform, but power consumption is high due to the low-Q inductor used. Tuning range, although greatly enhanced using the digital tune, is generally lower than the CMOS ring oscillators.

In this section is a brief discussion of the simulation results of the higher-frequency (2.45 GHz) oscillator, and the lower frequency oscillator follows the same pattern only at the lower frequency.

7.1.1 Tuning Characteristic

The tuning behaviour for the 2.45 GHz cross coupled oscillator is shown in fig. 7.1. The four tuning curves arise from different voltages applied at the digital
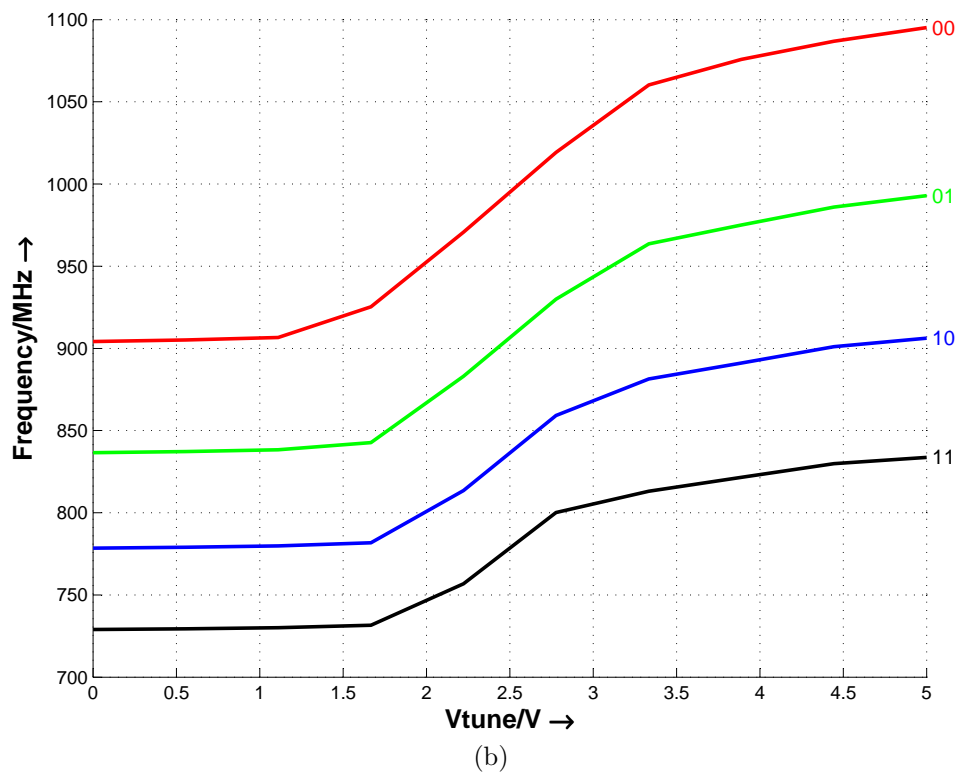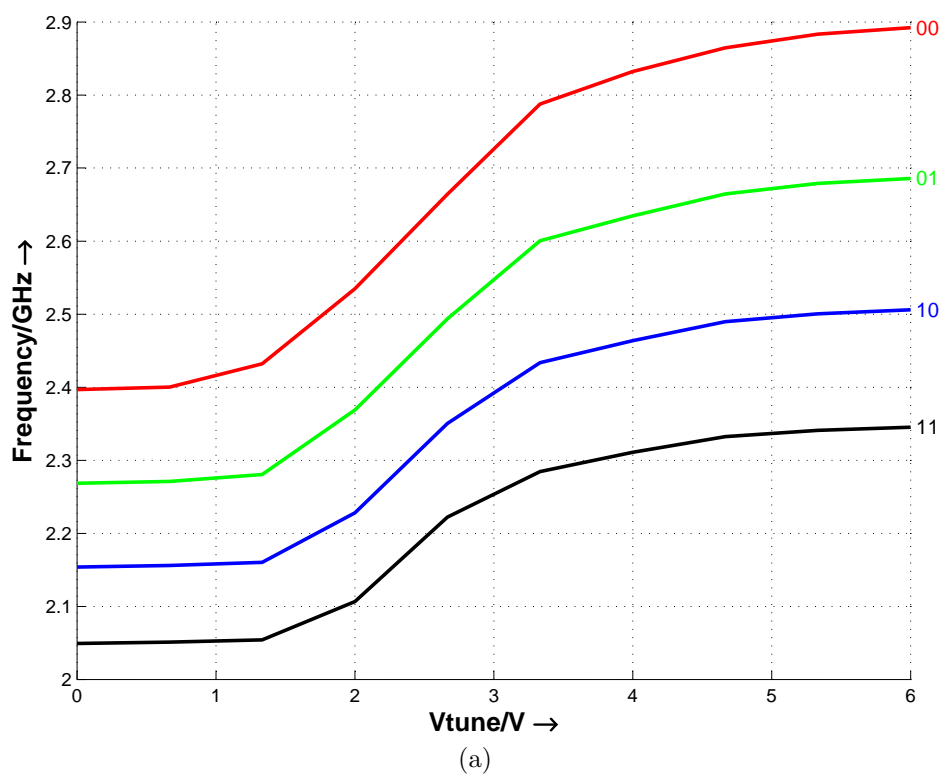
Figure 7.1: Tuning characteristics of the a) 2.45 GHz and b) 900MHz cross-coupled VCO.

tune inputs, which in this case are 2-bit, resulting in $2^2 = 4$ combinations and therefore four different tuning curves. At each digitally controlled frequency band, analog fine tuning is performed using the tuning varactors through a tuning voltage ranging from 0V → 5V or 6V. It is clear from the curves that analog tune is not linear over the whole tuning voltage range, but shows high linearity in the range from 1.5V → 3.5V. Tuning ratio is approximately 40% for the cross-coupled oscillators.

As mentioned in [15] and can also be observed from these tuning curves: The tuning sensitivity (or the slope of the tuning curve) of the analog-tune varactor component decreases at lower frequency bands. This happens simply because the change in capacitance caused by the varactor becomes a smaller fraction of the total capacitance after *switching-on* the digital-tune capacitors.

Overlap between the four tuning bands is an important parameter and is aimed in the design to be equal $\frac{1}{2}$. This could however never be the case for all frequency bands since each band displays a different K_{VCO}, not to mention parasitic components which are not taken into account in hand calculations or equations.

7.1.2 LO Waveform

The oscillator waveform is plotted in different digital-tune frequency bands and in the highest frequency band for different analog tune values (see fig. 7.2). It is observed that the amplitude of oscillation decreased at lower frequencies, when more switches and capacitors are connected in the oscillator. This phenomenon occurs because the oscillator Q decreases when more switches operate [15]; they introduce parasitic resistances in which some of the power becomes unintentionally dissipated.

The peak-to-peak voltage (V_{pp}) of the LO signal varied from approximately 3V → 5V across the 4 frequency bands. The highest V_{pp} is at the highest frequency band. This occurs because at this highest frequency band, no switches are operating, then as the tune value is incremented, more and more switches are turned-on. The switches are of course lossy, providing an explanation for the decrease in amplitude shown [15].

The buffer and driver stages were designed with gain = 1 so that the output of the entire transmitter also varied in the mentioned range of voltages. This is true for the unloaded simulated output but after loading with 50Ω resistors connected to ground (representing the measurement probes); the output voltage range dropped to the lower values of 0.8V → 1.7V. This is due to the current driving capability of the output stages. The simulated probes are placed as 50Ω resistors connected to ground since the output stage is a common-source amplifier, hence the ground connection.
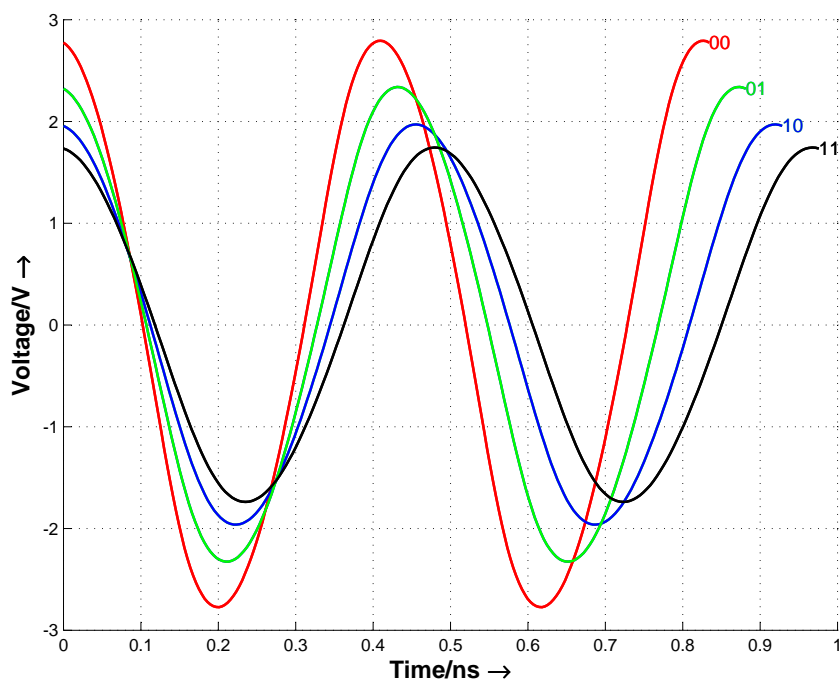
(a) LO waveform at the upper edge of the 4 tuning bands.
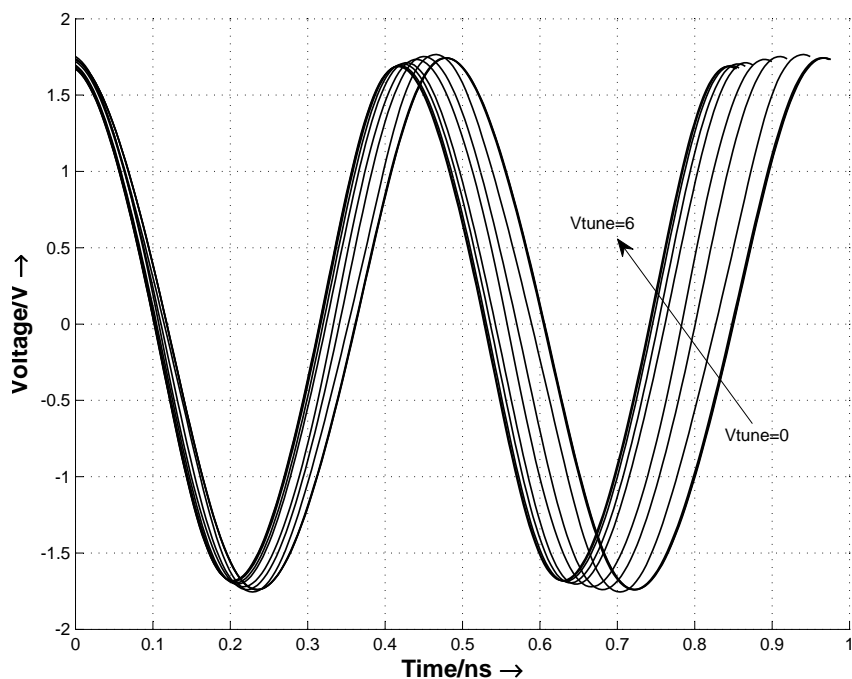
(b) LO Waveform vs. tuning voltage in the highest frequency band.

Figure 7.2: 2.45 GHz cross-coupled LO waveform as it varies with a) digital tune and b) analog tune.
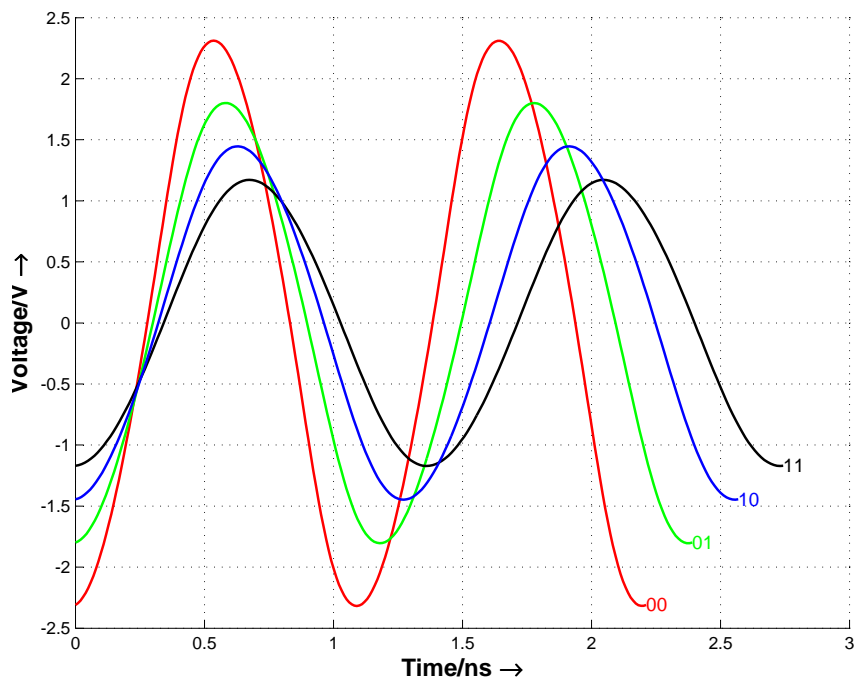
(a) LO waveform at the upper edge of the 4 tuning bands.
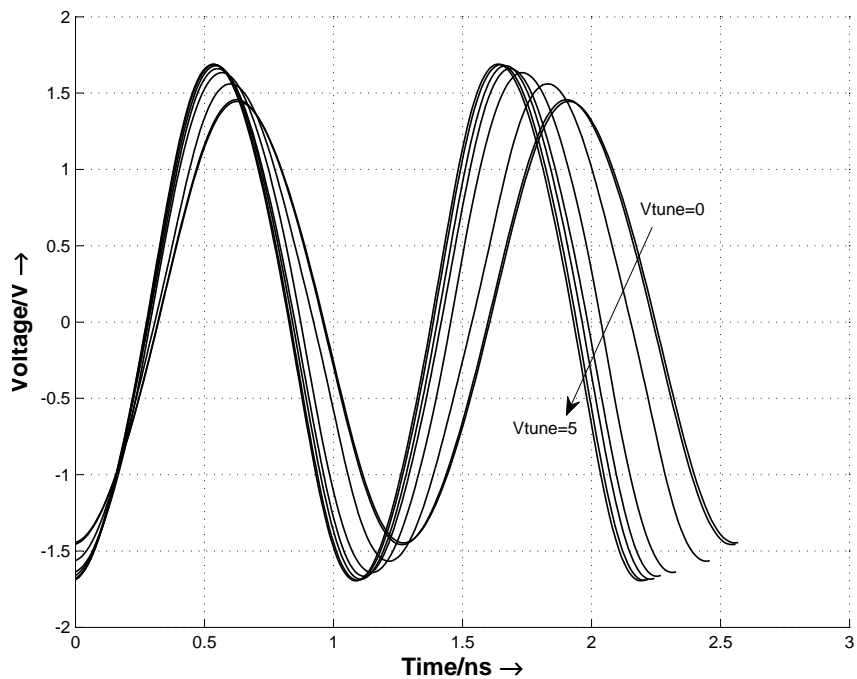
(b) LO Waveform vs. tuning voltage in the highest frequency band.

Figure 7.3: 900 MHz cross-coupled LO waveform as it varies with a) digital tune and b) analog tune.

7.1.3 Harmonic Spectrum

For the cross-coupled oscillators in general, and as expected, the waveform is a sinusoid with low harmonic components. This is shown in fig. 7.4. In the case of the 2.45 GHz oscillator, the nearest distortion harmonic component is less than -35 dBm thus indicating very good spectral purity.

The same could not be mentioned for the lower-frequency 900 MHz oscillator since that same harmonic component is -16 dBm, too large when compared to its 2.45 GHz counterpart. The reason behind this discrepancy in signal distortion between the two oscillators, although they share the same topology, is the size of the negative transconductance transistors, or the cross coupled pair. Cross coupling is the main source of noise in negative-g_m oscillators [5, 7], and larger transistors were used in the 900 MHz oscillator to provide more negative-resistance in order to compensate for inductor losses which increase at lower frequencies.

7.2 Differential Ring Oscillator

The differential ring oscillator has poor phase-noise performance when compared to the cross-coupled oscillator, but has a more compact design and lower power dissipation. A summary of the simulation results follow, transient simulations were run on this oscillator circuit.

7.2.1 Tuning Characteristic

Oscillation frequency is tuned through current steering, this makes the frequency changeable from DC to the highest possible in the ring oscillator chain, which in this case is approximately 1.2 GHz. Since CMOS topology is used, the output waveform amplitude does not vary greatly when the tuning current is changed.

The ring oscillator is very sensitive to tuning current, and it shows a very high K_{VCO} of approximately 325 MHz/mA, this is why it is of high importance to place the RC filters discussed earlier.

As it can be observed from the tuning curve in fig. 8.8, the tuning linearity is quite poor. The tuning characteristic is *curved* and the K_{VCO} decreases with increasing frequency, the reason behind this is not investigated. It is possible to get a linear range, however, by tuning only between 200 MHz and 1 GHz where the tuning curve shows fairly good linearity.
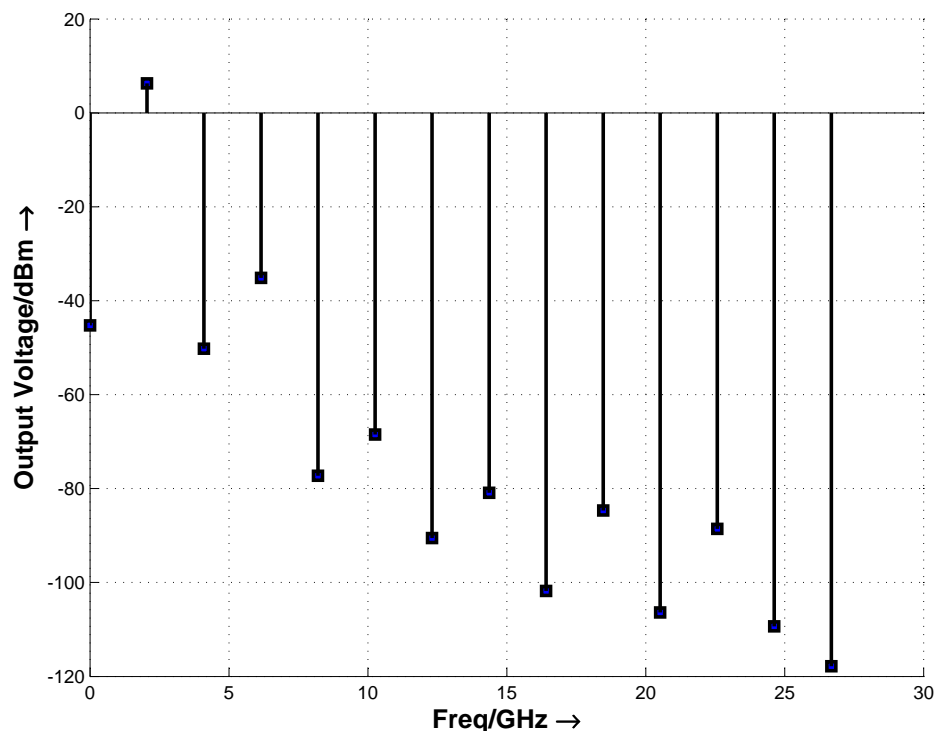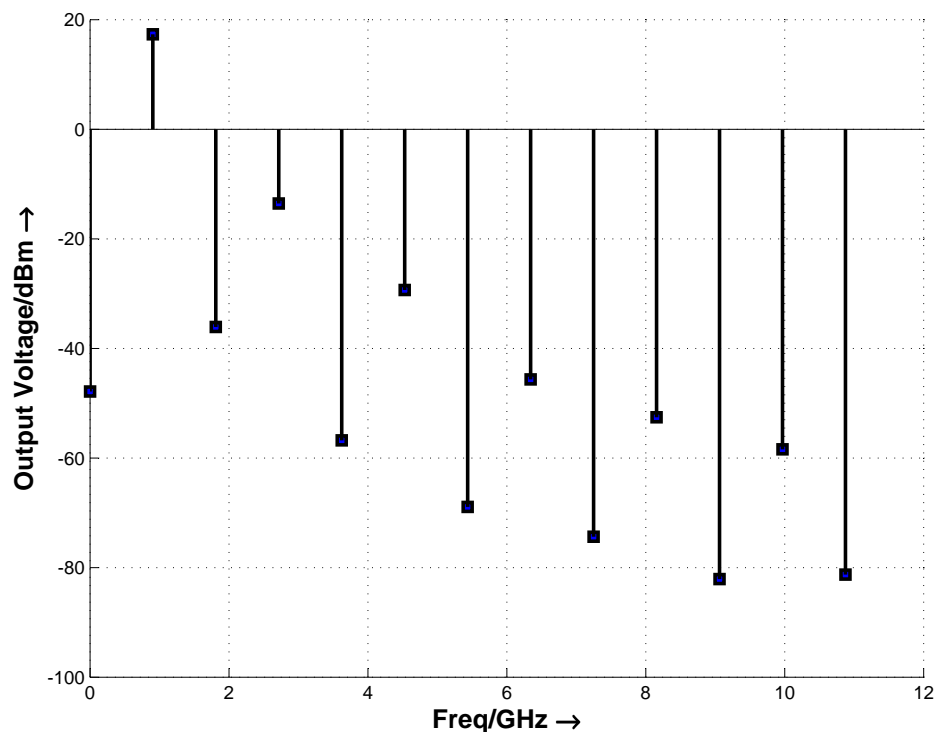
Figure 7.4: LO harmonic spectrum of the a) 2.45 GHz and b)900 MHz cross-coupled oscillator.
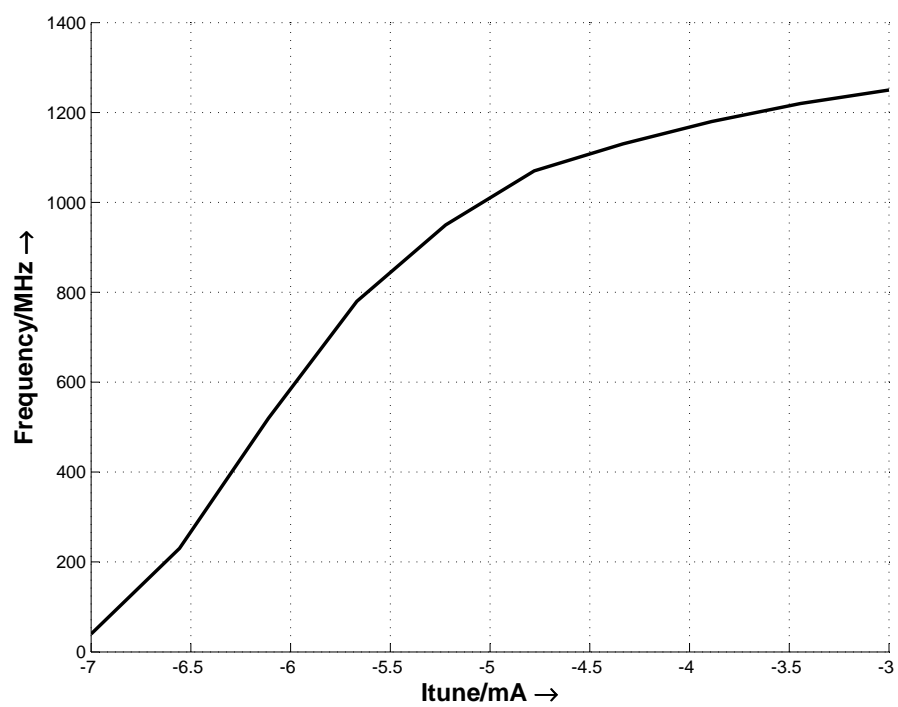
Figure 7.5: Differential ring oscillator: Output frequency as a function of tuning current.

7.2.2   Output Waveform

In fig. 7.6 is the simulation of ASK modulation input with a data rate of 100 MHz
and the output waveform is displayed on the same plot showing the variation in
amplitude that resulted. The ASK voltage high is 5V and the low represented by
2.5V, this is required for correct operation. The ASK modulation ratio is about
0.3:1 for the low:high input ASK values respectively.

The output waveform is not purely sinusoidal, it suffers from high distortion
components, but this is expected for the ring oscillators, especially those used
since there were no capacitors in between to smooth the waveform. Fig. 7.7
shows a closer look on the output voltage which had V_{pp} of about 2 volts. This is
the output as it is after loading with the 50Ω resistors (representing the probes)
at the output, also connected to ground as it is the case with the cross-coupled os-
cillators. The LO waveform had a larger voltage swing; about 8 volts differential
peak-to-peak.

Figure 7.6: Differential ring oscillator: ASK modulation and how it varies the
output waveform amplitude.
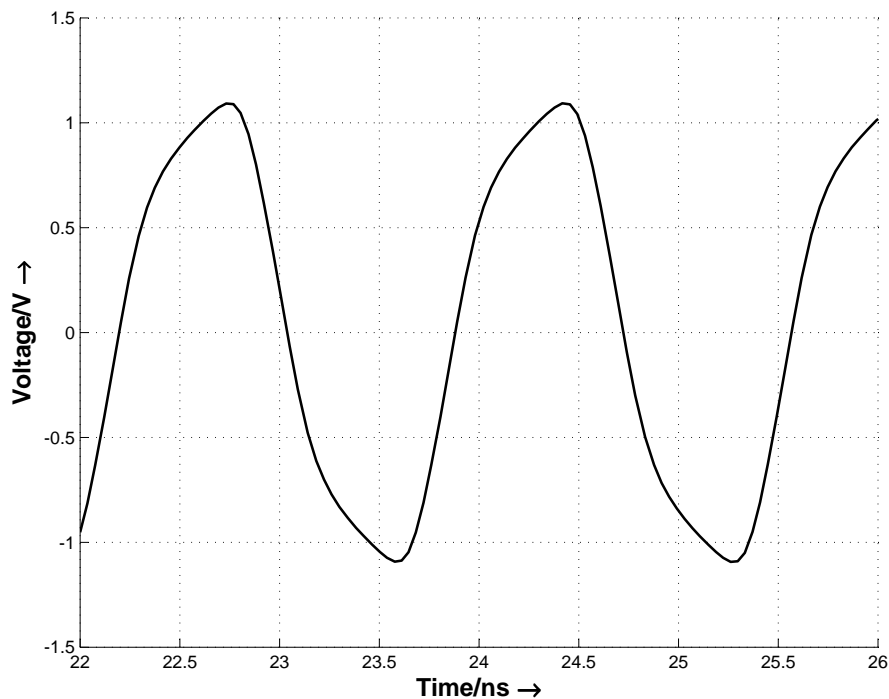
Figure 7.7: Differential ring oscillator: Output waveform.

7.2.3   Harmonic Spectrum

The harmonic spectrum is calculated for the oscillator from transient simulations by applying fourier series analysis on the output voltage waveform, resulting in the plot shown in 8.10. The output waveform had poor spectral purity as can be seen from its frequency components, the fundamental frequency had a magnitude of 20 dBm, and the nearest harmonic has the very high value of 7 dBm, the next harmonic: -10 dBm. This poor spectral purity is also displayed through the shape of the output in fig. 7.7.

7.3   Single-ended Ring Oscillator

An advantage present in differential topologies is the filtering of common-mode noise, since the differential outputs are subtracted to result in the output, and noise usually affects both the positive and negative outputs equally. This advantage is already not present in single-ended topologies therefore it is expected to have degraded noise performance.
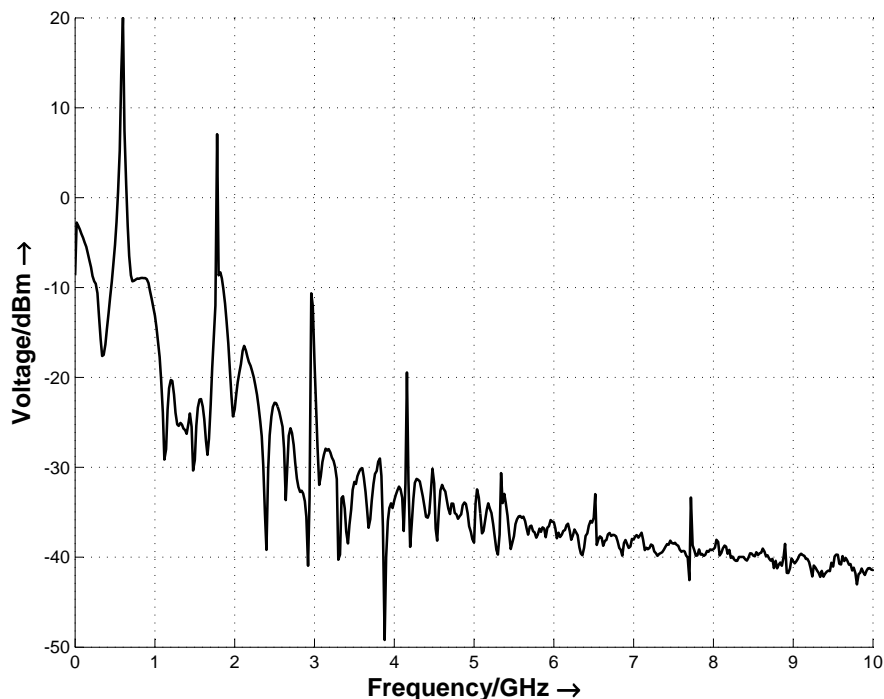
Figure 7.8: Differential ring oscillator: Output signal harmonic spectrum.

7.3.1 Tuning Characteristic

This circuit is designed to operate at the lower frequency of 433 MHz (ISM band), this is why it is sufficient to have a tuning range that reaches a maximum of 900 MHz. Seven stages of inverters were used to arrive at this frequency range, without the use of any intermediate capacitances. The tuning curve is shown in fig. 8.11. As before in the differential ring oscillator, this oscillator is frequency controlled by steering of the inverters' tail currents. Because this too is a CMOS inverter, the output voltage swing does not degrade greatly with the frequency tune.

From the plot in fig. 8.11 the following can be observed: the tuning curve is not of high linearity but shows an acceptable response which has higher linearity than the differential ring oscillator discussed before. The tuning range is from below 100 MHz up to 800 MHz, and the tuning sensitivity is quite high, about 210 MHz/mA. K_{VCO} is smaller than that of the differential ring oscillator since the range is already smaller for the same tuning current range.
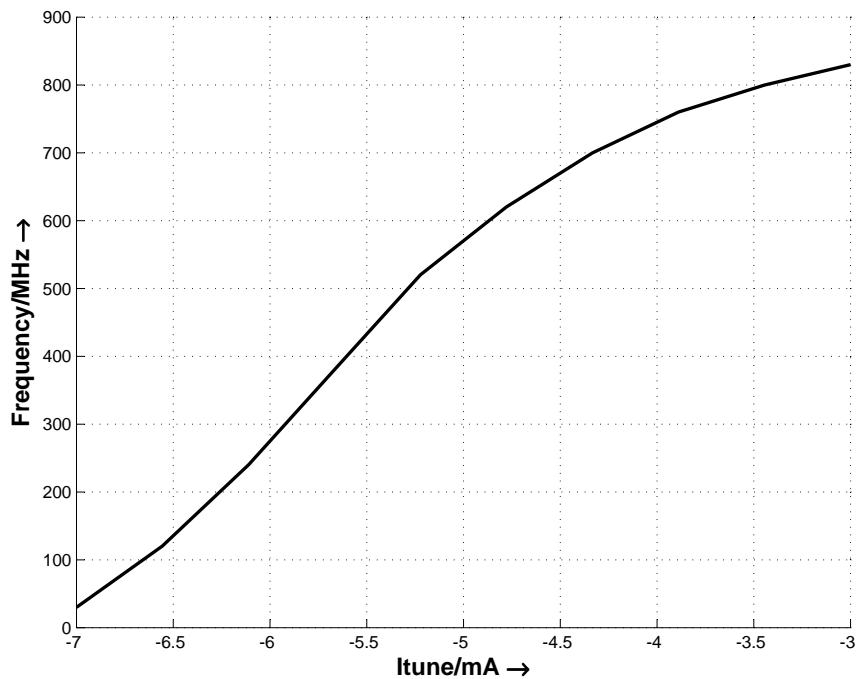
Figure 7.9: Single-ended ring oscillator: Output frequency as a function of tuning current.

7.3.2 Output Waveform

ASK modulation input is implemented simply as a pull-to-ground NMOS transistor at the output, when properly sized with respect to the pull-up PMOS transistor of the output stage; ASK modulation ratio could be chosen. This is clear from fig. 7.10 where a high modulation input causes a decrease in output waveform and vice versa. When a high input is placed on the NMOS modulation transistor, it is switched on and the signal is *pulled* to ground, this is why the effect of modulation is opposite to what is expected, but this makes no difference in circuit operation, an inverter could simply be placed at modulation input to invert the values.

The output, similar to that discussed in the differential ring oscillator, is also distorted because of the use of many inverter stages (7) with no intermediate capacitors. The waveform shown here is at the output after loading with the 50Ω resistors (simulating the measurement probes). The LO output however had a rail-to-rail output from V_{DD} to V_{SS}.
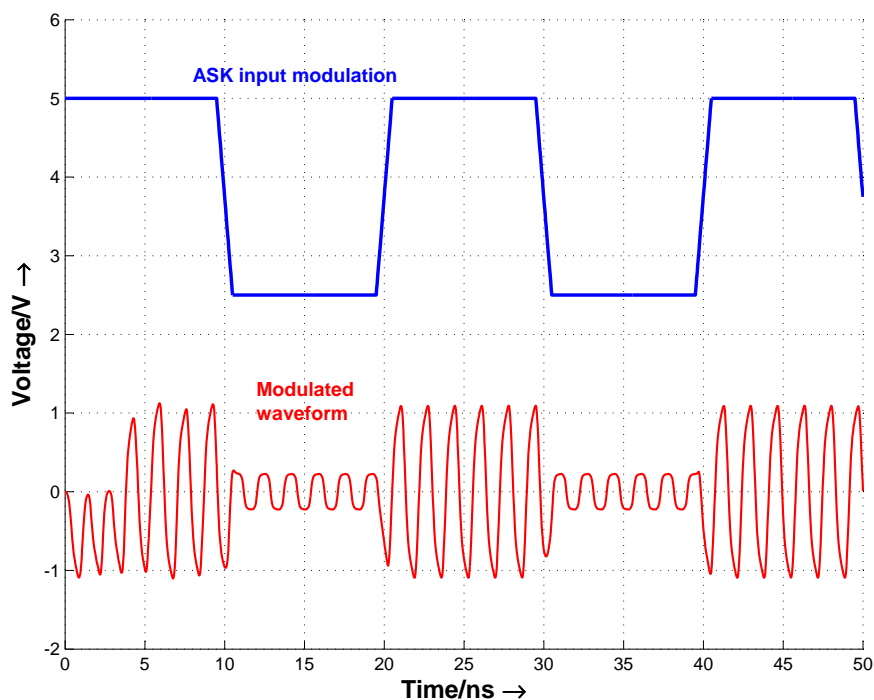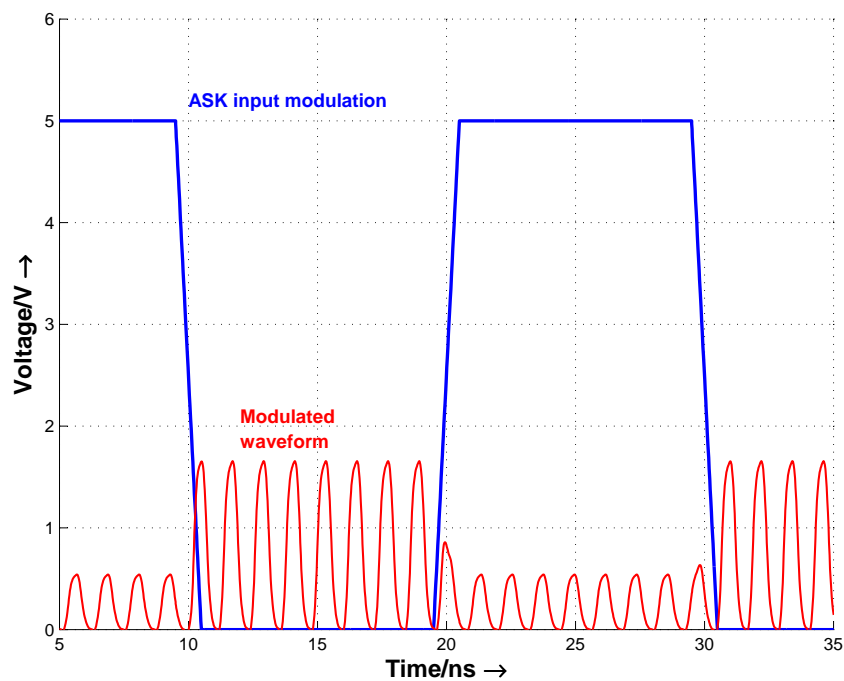
Figure 7.10: Single-ended ring oscillator: ASK modulation and how it varies the output waveform amplitude.
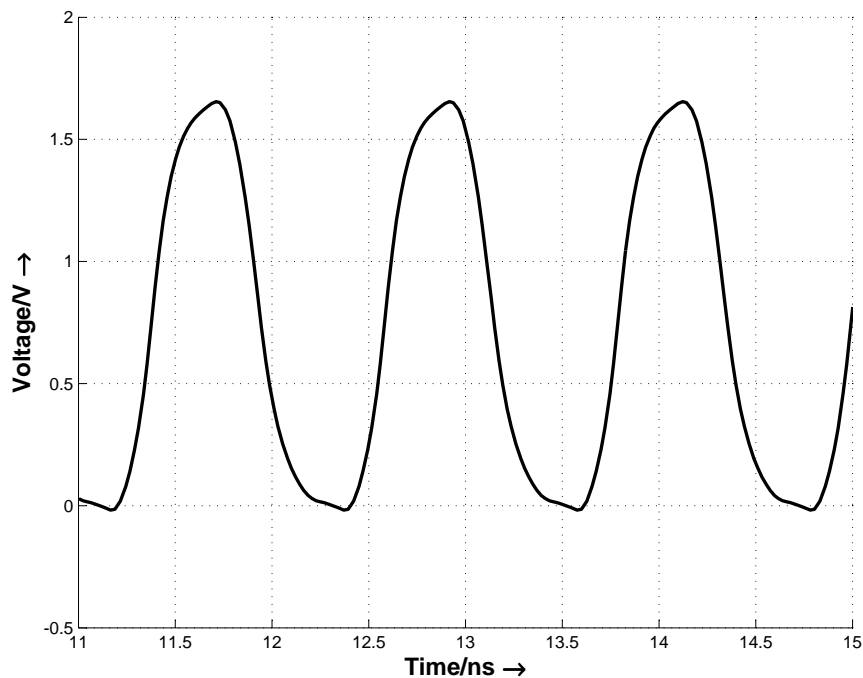
Figure 7.11: Single-ended ring oscillator: Output waveform.

7.3.3   Harmonic Spectrum

The harmonic spectrum shown in fig. 8.13 is quite poor, but expected; as it is clear from the output waveform, the signal is quite distorted with low spectral purity. Similarly to the differential implementation, the fundamental frequency component is about 20 dBm followed by harmonics at 6 dBm then -6 dBm.
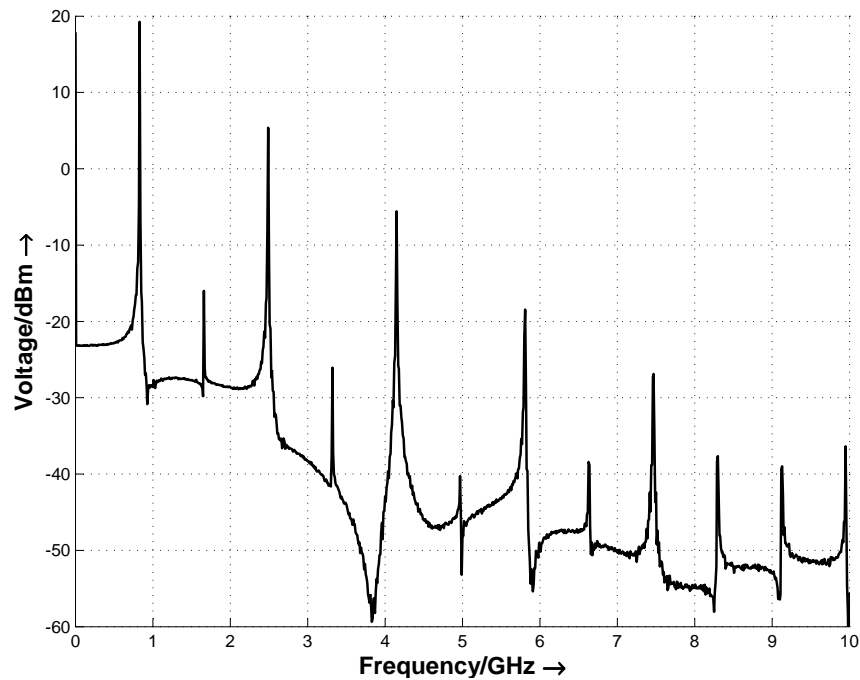
Figure 7.12: Single-ended ring oscillator: Output signal harmonic spectrum.

Chapter 8

Measurement Results

After Fabrication of the test VCO structures, measurements are conducted to verify the simulation results and to assert the possibility of implementing RFID on this gate-array technology. This chapter discusses the measurement results and provides a comparison to the attained simulation results, and possible reasons behind the observed descripancies. First the measurement setup is described, then the results of each VCO are seperatly presented.

8.1   Measurement Setup
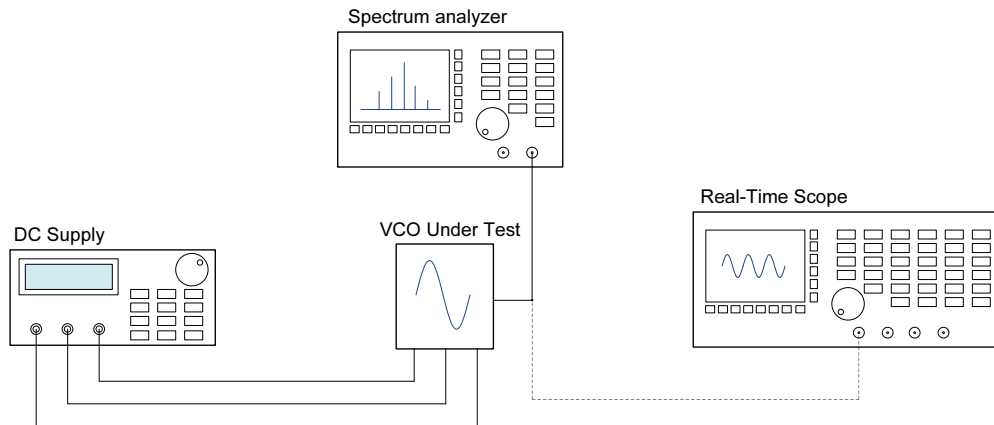
Figure 8.1: Abstraction of the employed measurement setup.

The measurement setup shown in fig. 8.1 is used to extract the VCO behaviour. The input to the VCOs is comprised of only DC signals for biasing the circuitry and control of the tune inputs to vary the frequencies, for

that, only DC supplies were used. A maximum of two DC supplies were required to be able to have enough degrees of freedom in varying all the parameters. The power consumption was also evaluated using the power supplied by utilizing their built-in multimeters used for current measurement, and $Power(p) = Voltage(V) \times Current(I)$.

Of highest importance was measuring the VCO output frequency spectrum. The Rhode & Schwarz FSL frequency spectrum analyser (3 GHz) was used for this purpose. Only a single output of the diffrential amplifiers was analysed with the other output terminated with 50Ω. These output measurements were used to plot the tuning characteristic curves and to analyze the noise behaviour of the output signal as well.

To verify the output signal shape and to accurately measure the amplitude of the output signal, the Tektronix TDS694C real-time scope (10 G/s) was used. Using this measurement device, the sinusoidal output signal was plotted, from which the amplitude was evaluated. Note that in fig. 8.1, this device is connected with a dotted line, this is to signify that either the real-time scope or the spectrum analyzer were connected during a measurement, not both. It is also worthy to note that when a DC block was connected between the VCO and the scope, the output signal deteriorated significantly. This occurs because a DC block disturbs the biasing point of the output amplifier thereby driving it out of the correct operating point. This conforms with simulation.

8.2   Cross-coupled 2.4 GHz VCO

The tuning curves of the 2.45 GHz cross-soupled VCO are shown in fig. 8.2. The expected shape was obtained as can be seen, with 4 tuning curves of approximately equal spacing between each curve and the next. The tuning frequency varied from 1.755 GHz to 2.155 GHz. One can immeadiately realize that the results do not agree with simulation, which ranged between 2.0 GHz - 2.95 GHz, the deviation for this specific VCO was rather high, as was expected, since it is the one operating at the highest frequency.

Fig. 8.3 shows the real-time scope signal attained from the second measurement. It is clear that the output signal is a sinusoid, with good spectral purity. The peak-to-peak voltage meaured at the top frequency was 350 mV and at the lowest frequency it was approximately 400 mV. This decrease of voltage with the increase in frequency is also what was attained from simulation.

Fig. 8.4 presents two snapshots of the frequency spectrum from the 2.45 GHz cross-coupled VCO; the highest and the lowest frequencies (they can be directly read from the plot).
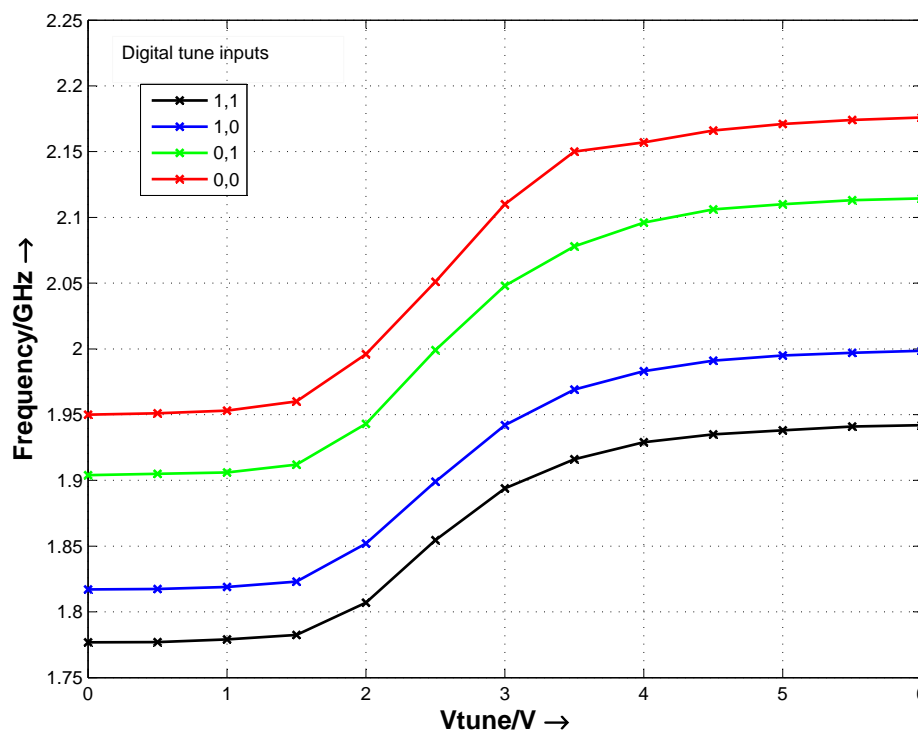
Figure 8.2: Tuning characteristics of the 2.45 GHz cross-coupled VCO.
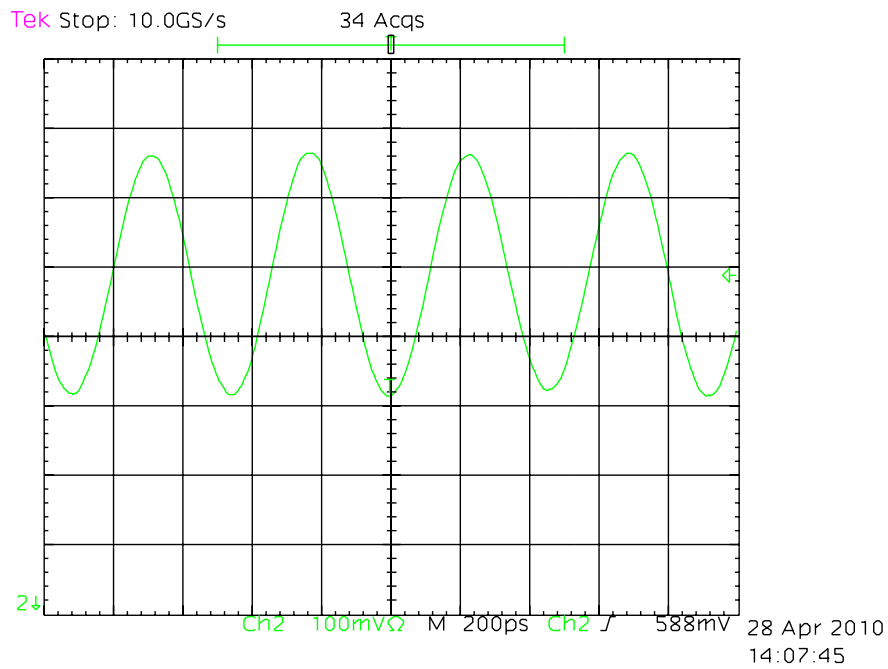
(a)
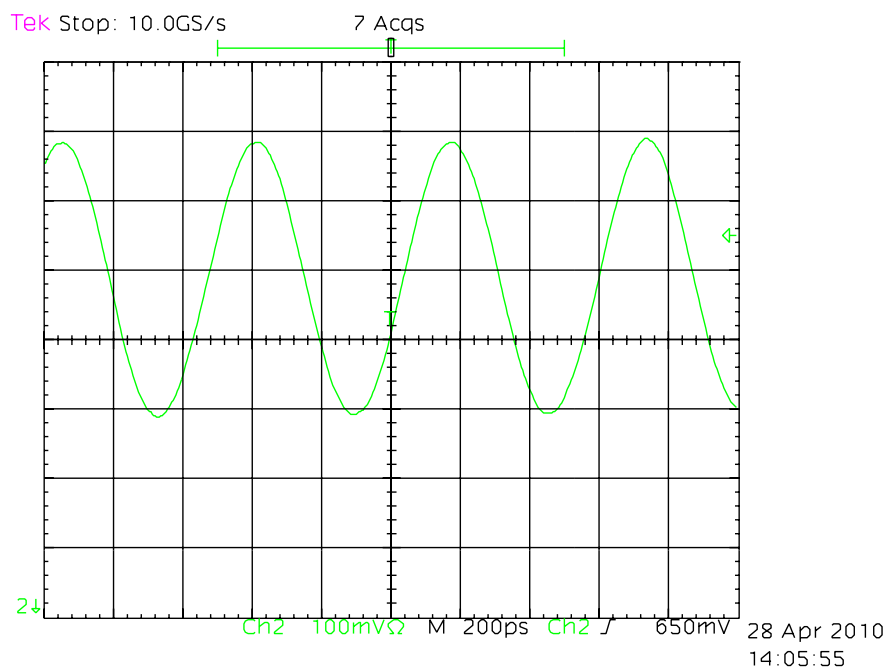
(b)

Figure 8.3: Real-time scope snapshot of the waveform of the 2.45 GHz cross-coupled VCO at a) the highest and b) lowest frequencies of operation.
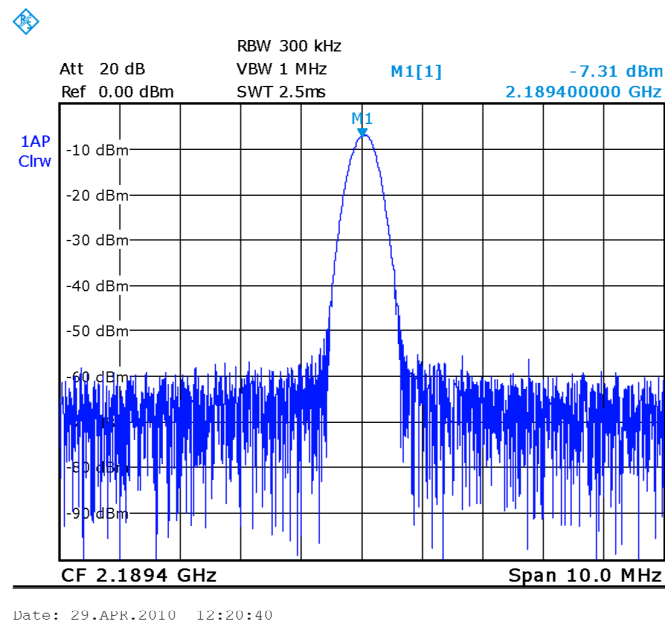
(a)
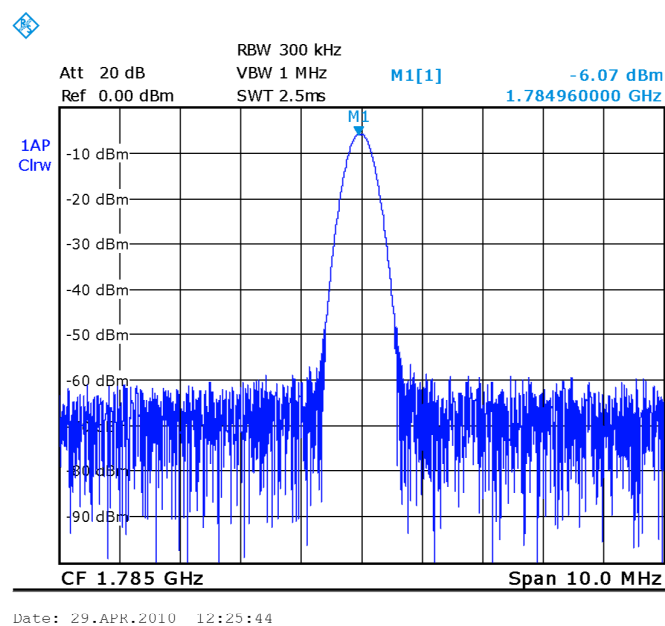
(b)

Figure 8.4: Measured output spectrum of the 2.45 GHz cross-coupled oscillator at a) the highest and b) lowest frequencies of operation.

8.3   Cross-coupled 900 MHz VCO

The tuning curves of the 900 MHz cross-soupled VCO are shown in fig. 8.5. The expected shape was obtained as can be seen, with 4 tuning curves of approximately equal spacing between each curve and the next. The tuning frequency varied from 0.82 GHz to 1.19 GHz. The results aren't exactly the same as in the simulation, but the deviation is small compared to the 2.45 GHz VCO. The curves are shifted downwards by about 50 MHz when compared to simulation and they retain the same shape.
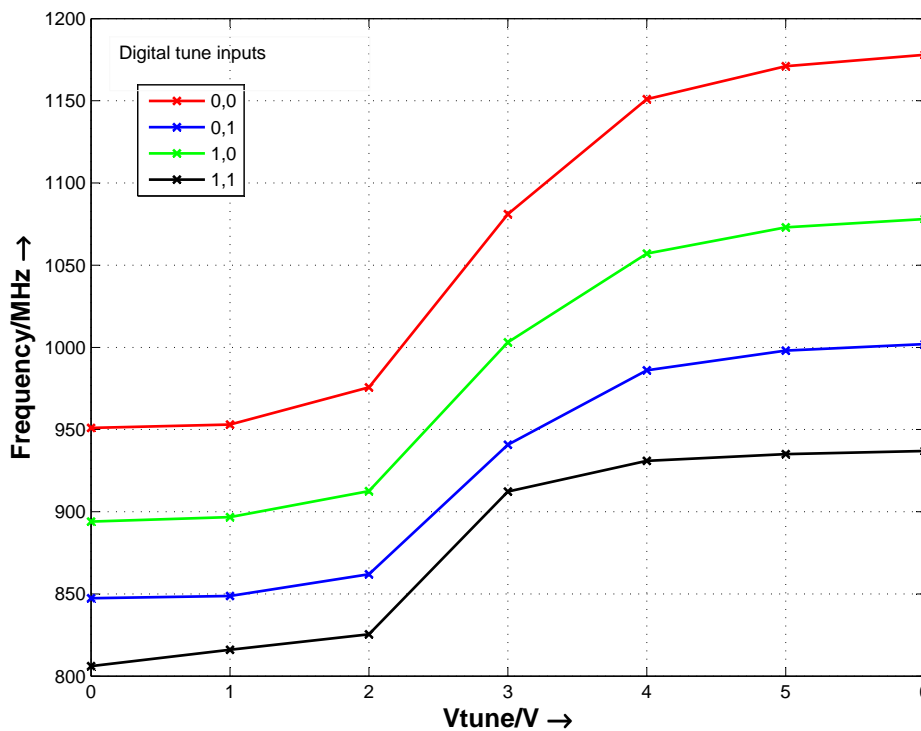
Figure 8.5: Tuning characteristics of the 900 MHz cross-coupled VCO.

Fig. 8.6 shows the real-time scope signal for the 900 MHz VCO. It is clear that the output signal is a sinusoid, with good spectral purity. The peak-to-peak voltage meaured at the top frequency was 650 mV and at the lowest frequency it was approximately 580 mV. This increase of voltage with the increase in frequency was not expected, further investigation is required to find the reason behind this.

Fig. 8.7 presents two snapshots of the frequency spectrum from the 900 MHz cross-coupled VCO; the highest and the lowest frequencies (they can be directly read from the plot).
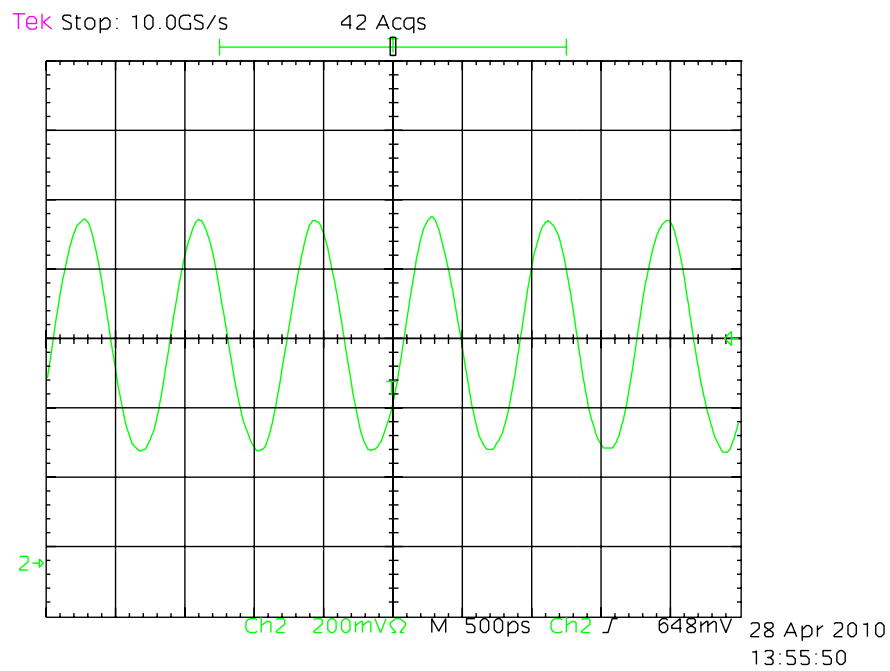
(a)
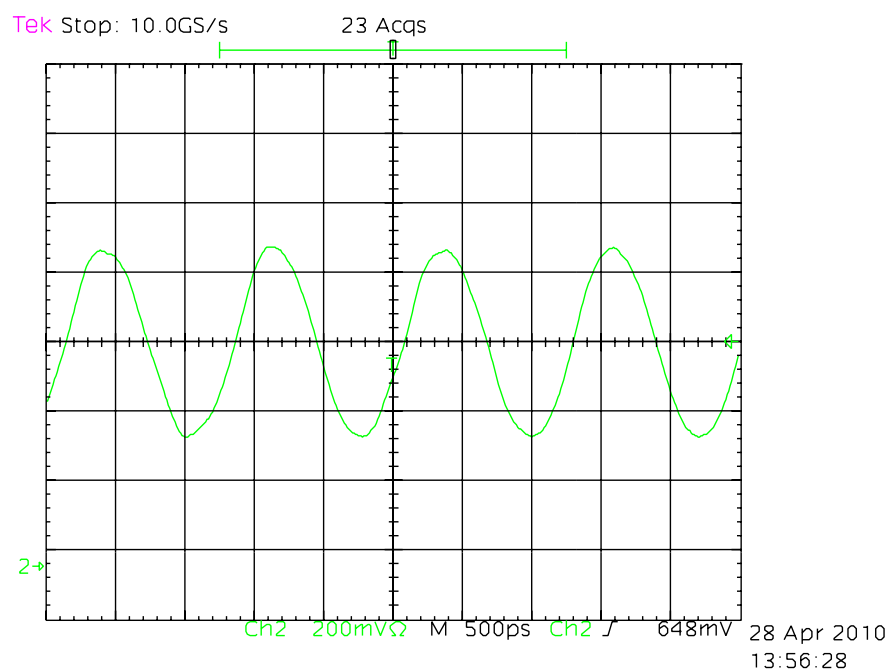
(b)

Figure 8.6: Real-time scope snapshot of the waveform of the 900 MHz cross-coupled VCO at a) the highest and b) lowest frequencies of operation.
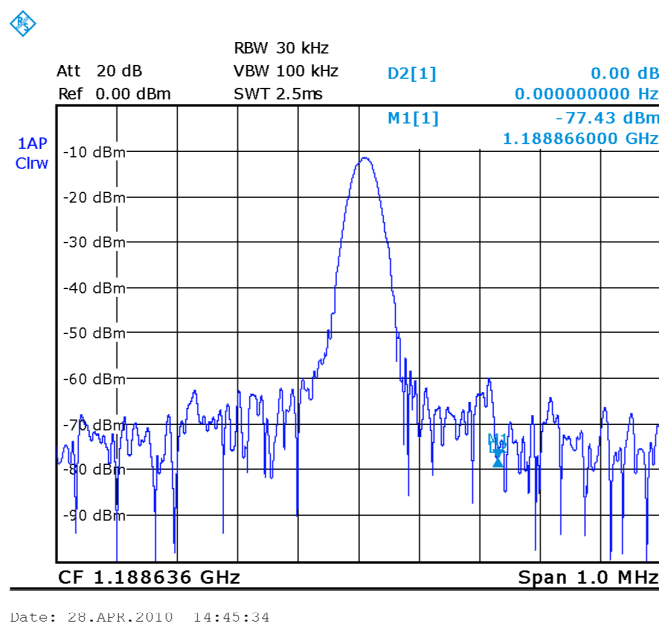
(a)
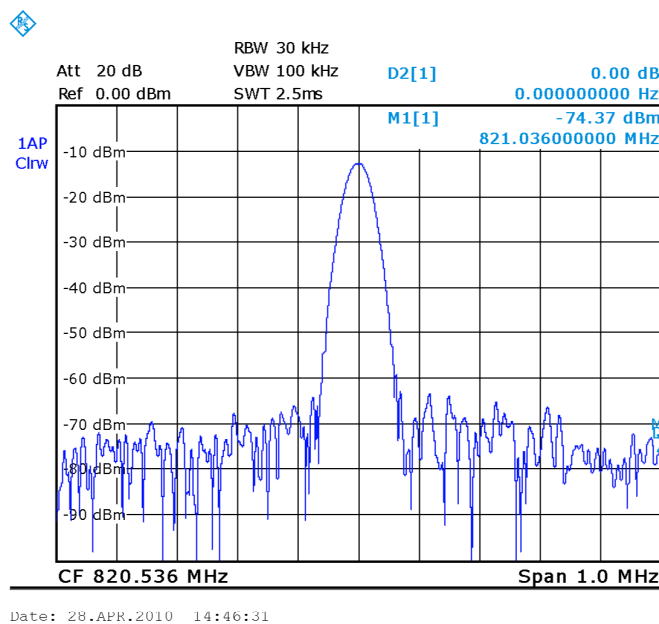
(b)

Figure 8.7: Measured output spectrum of the 900 MHz cross-coupled oscillator at a) the highest and b) lowest frequencies of operation.

8.4   Differential Ring VCO

The frequency measurements of the differential VCO compiled into the tuning curves are shown in fig. 8.8. The plot is different from the one presented in simulation results since the simulated plot was plotted versus tuning current while measurements were done by varying voltage. Simulated top frequency was about 1200 MHz compared to the 950 MHz obtained from measurements.
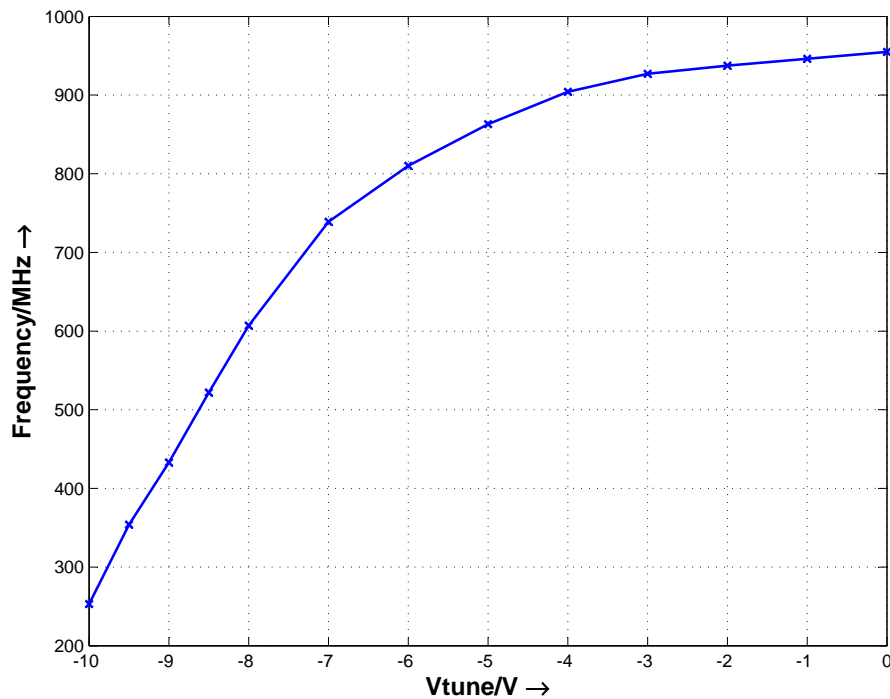
Figure 8.8: Differential ring oscillator: Output frequency as a function of tuning current.

The real-time scope recorded the signal shown in fig. 8.9 for the differential ring oscillator. The signal is a non-ideal sinus, the higher-order harmonics are the reason for that. However it is expected that the ring oscillator produces such output and it is similar to simulation results. Measured peak-to-peak voltage is approximately 0.65 V.

Fig. 8.10 presents a snapshot of the measured frequency spectrum from the differential ring VCO.

Tek Stop: 10.0GS/s   15 Acqs

Ch2 200mVΩ   M 500ps Ch2 ∫   848mV   28 Apr 2010
                                                14:48:40

Figure 8.9: Real-time scope snapshot of the waveform of the differential ring VCO.
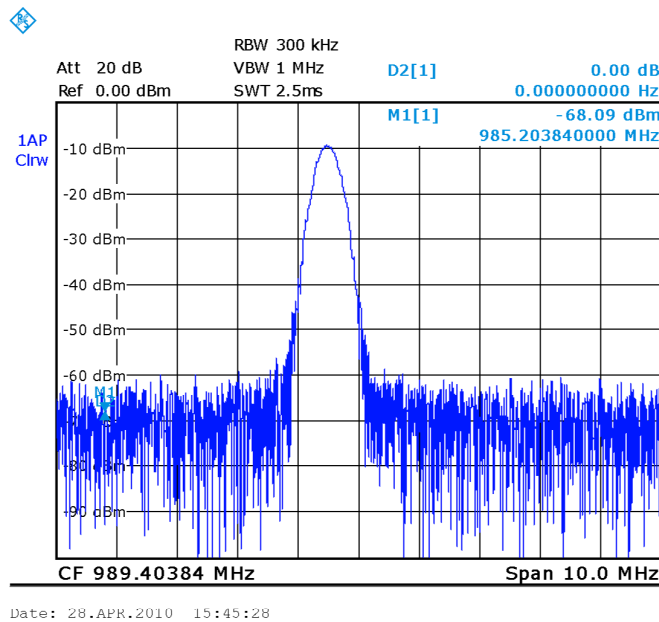
Figure 8.10: Measured output spectrum of the differential ring oscillator.

8.5   Single-Ended Ring VCO

The frequency measurements of the single-ended VCO compiled into the tuning curve shown in fig. 8.11. The plot is different from the one presented in simulation results since the simulated plot was plotted versus tuning current while measurements were done by varying voltage. Simulated top frequency was about 830 MHz compared to the 790 MHz obtained from measurements. This is the smallest offset in frequency for any of the oscillators, the results are further discussed in the following section.
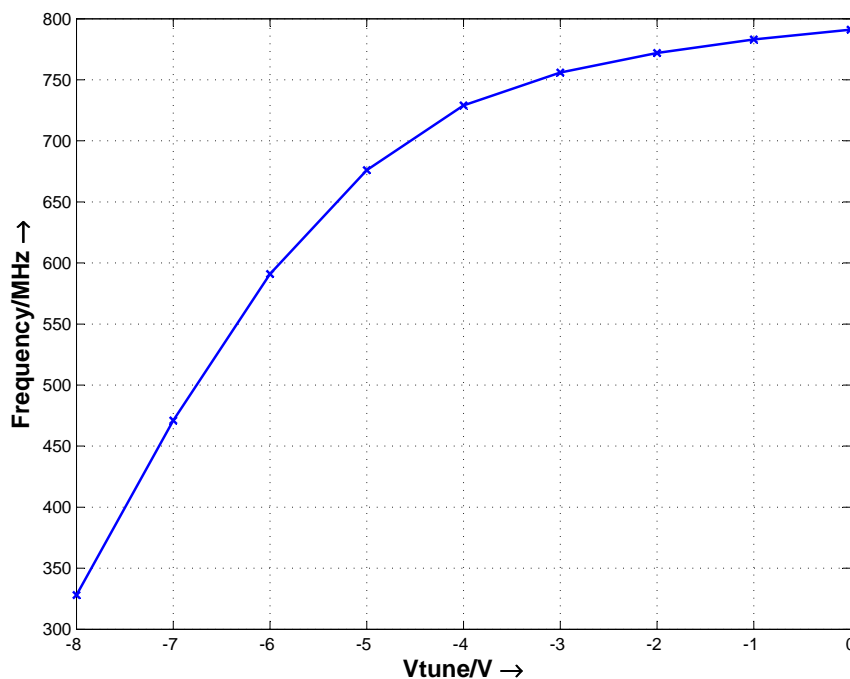
Figure 8.11: Single-ended ring oscillator: Output frequency as a function of tuning current.

The real-time scope recorded the signal shown in fig. 8.12 for the single-ended ring oscillator. Here, the harmonics' effect is apparent, as we have a non-ideal signal of low spectral purity. However it is expected that the ring oscillator produces such output and it is actually quite similar to simulation results. Measured peak-to-peak voltage is approximately 0.45 V.

Fig. 8.13 presents a snapshot of the measured frequency spectrum from the single-ended ring VCO.
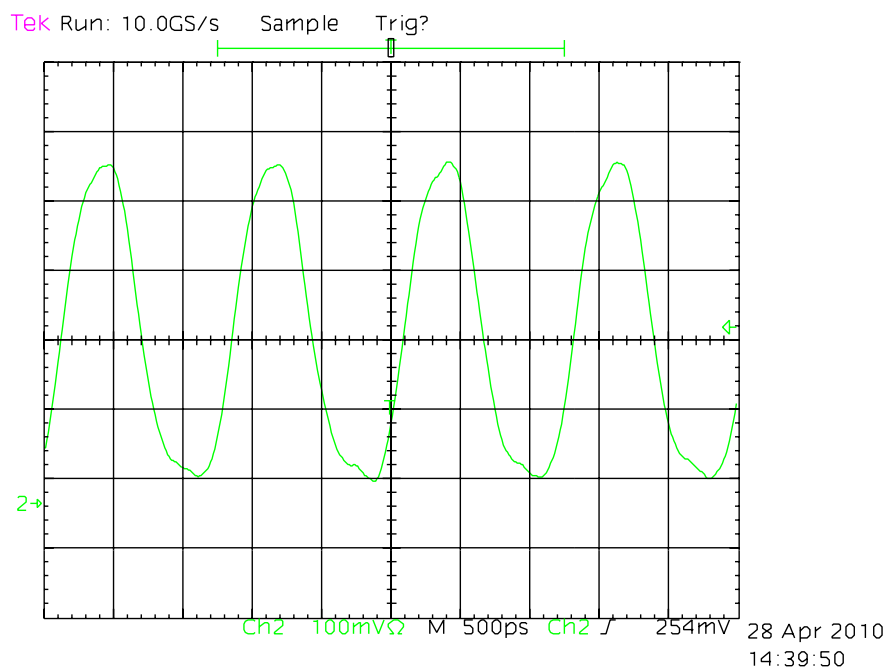
Figure 8.12: Real-time scope snapshot of the waveform of the single-ended ring VCO.
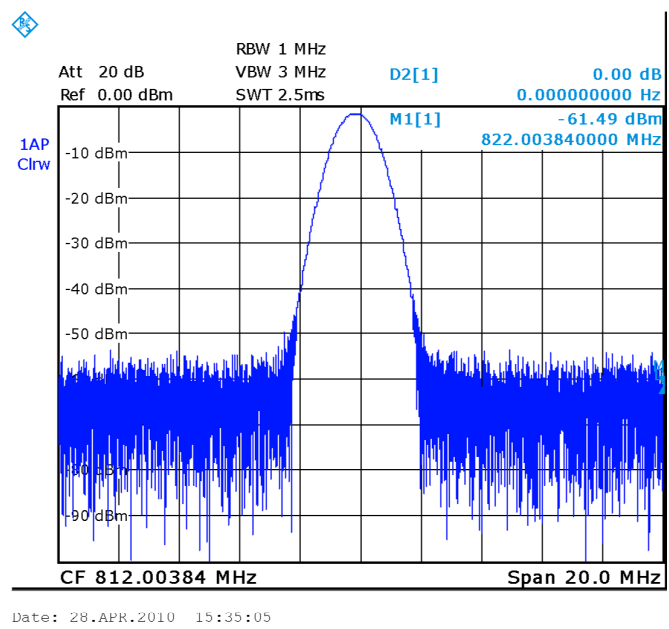
Figure 8.13: Measured output spectrum of the single-ended ring oscillator.

8.6   Summary of measurement Results

Measurements generally showed positive results for integration of an RFID on the new technology. All the designed VCOs operated as expected with some shifts in frequency due to parasitics that were unaccounted for. That aside, the transmitters displayed behaviour that is as expected from simulation. In addition, frequencies above 2.1 GHz were achieved with cross-coupled VCO, and a tuning ratio of up to 40% could be reached with the other cross-coupled VCO.

The simulation and measurement results did not match completely.There was a clear frequency difference between simulation and measurements. After investigation, that was found out to be due to underestimation of the parasitic silicon substrate capacitance. This effect was highlighted because the VCOs operating at the higher frequency experienced a greater deviation from simulated results. Furthermore, the wiring used did not have a high value of total resistance ruling that out as a factor in the differences between measurement and simulation. In addition, the silicon substrates in general are known to be lossy when integrating such devices as inductors on them, this is due to the low resistivity of the silicon substrates, this phenomenon is discussed further in chapter 2. To rectify this issue, a more accurate parasitic extraction from layout has to be done before final simulations, it is safer to use a more pessimistic model for the inductor as well.

Another obvious discrepancy between simulation results and measurements was the power consumption. Measured power consumption was lower than expected for the three oscillators that used a CML stage as an output driver in which the amplitude is also lower than simulated. The reason for this is either mismatch in the biasing circuit or due to the wiring resistan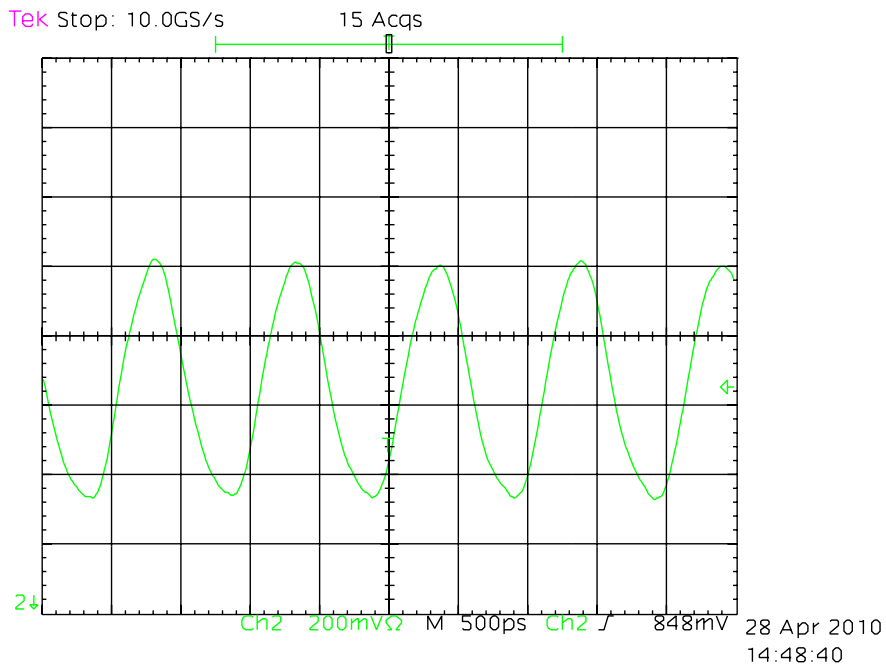ce that was unaccounted for, which resulted in lower power being delivered to the driver. By increasing the operating voltage of the circuits this can be compensated. On the other hand, the CMOS output stage used in the ring oscillator consumed more power than expected while still producing a smaller output amplitude. In this case, the reason is the parasitic capacitance between CMOS stages in the output amplifier. This leads to a higher dynamic power dissipation as well as increased short-circuit power while switching, since a higher load capacitance means slower switching.

For reliability of measurement data, the measurements were performed on more than one chip. It was found that the variation between chips was minimal as clarified by table 8.2 in which the maximum frequency of the 2.45 GHz cross-coupled oscillator was measured and chosen for comparison. The difference between the highest and lowest frequency was abut 22 MHz which corresponds to less than 1% variation with respect to the maximum frequency.

	Feature	Cross 2.45GHz	Cross 900MHz	Diff. Ring	Single Ring
Power	Simulated Power	163 mW	196 mW	180 mW	76 mW
	Measured Power	100 mW	130 mW	150 mW	250 mW
Tuning	Simulated Range	2.0-2.95 GHz	730-1100 MHz	0-1200 MHz	0-900 MHz
	Measured Range	1.775-2.175 GHz	800-1175 MHz	250-950 MHz	300-800 MHz
	Simulated Ratio	39%	41%	-	-
	Measured Ratio	20%	42%	-	-
Output	Simulated V_{pp}	1 V	1.4 V	2 V	1.4 V
	Measured V_{pp}	0.4 V	0.6 V	0.65 V	0.45 V

Table 8.1: Comparison of simulation and Measurement Results.

chip number	Max frequency [GHz]
1	2.2004
2	2.1781
3	2.1839
4	2.1826
5	2.1826
6	2.1970
7	2.1898
8	2.1900

Table 8.2: Variation of maximum frequency of the 2.45 GHz cross-coupled VCO across 8 different chips.

8.7 Extraction and Resimulation of Parasitic Capacitance

To reason for the difference between measured and simulated frequency of operation, especially in the 2.4 GHz cross-coupled VCO, the parasitic capacitance of the layout structure is investigated. Using the simple parallel plate capacitor model, the additional parasitic capacitance due to the thick metal wires used on the oscillation nodes is calculated. This capacitance is clarified in fig. 8.14.

The equation for a parralel-plate capacitor is:

$$C = \epsilon_0 \epsilon_r \frac{A}{d} \tag{8.1}$$

- ϵ_0 is the permitivity of free space, $\epsilon_0 = 8.85 \times 10^{-12} m^{-3} kg^{-1} s^4 A^2$.

- ϵ_r is the relative permetivity of the borophosphsilicate glass used as passivation between metal layers, $\epsilon_r = 3.4$.

- A is the area of the wire, it is measured from the layout for each oscillation node: $A = 29043 \mu m^2$.

- d is the distance between the metal layer and the ground, which is calculated as the interface between the glass and the substrate, $d = 1400 nm$.

From these parameters the parasitic capacitance is estimated at $C_{par} = 715 fF$ on each of the hot nodes. When the circuit was resimulated using this parasitic capacitance the maximum operating frequency was shifted from 2.9 GHz to 2.267 GHz. This is much closer to the measured value of 2.175 GHz.

It is therefore concluded that the reason for the difference in measured and simulated frequency is due to the parasitic capacitance which was greatly underestimated and showed a strong effect especially in the highest-frequency oscillator. The discrepancy was apparent in the 2.4 GHz VCO since the parasitic capacitance was comparable in value to the capacitor value used in the LC tank unlike the 900 MHz VCO in which the capacitance used was much larger than the parasitic capacitance.
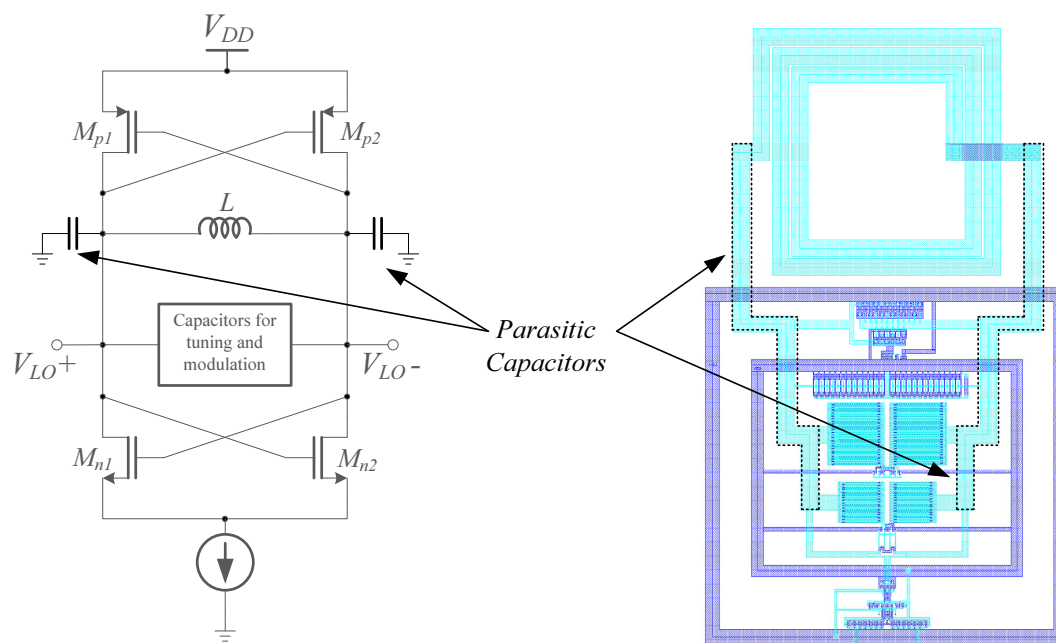
Figure 8.14: Parasitic capacitance shown on schematic and layout of 2.4 GHz cross coupled VCO.

Chapter 9

Layout

In designing the physical layout of a circuit a lot of different factors must be taken into consideration. In some circuits it may be most important to design for small chip area, while in other circuits it is symmetry that becomes the deciding factor. In this chapter the basic concepts used in designing the layout for the designed circuits are summarized, then a detail of each layout block is presented.

9.1 Analog layout

The main design points that constraint the freedom when designing a circuit's physical layout are summarized in the following list[20]:

- Area
- Symmetry
- Isolation
- Floorplanning
- Matching
- Device splitting
- Wire widths
- Parasitics
- Overlap
- I/O pads

The main points from above, and how they applied to this work are now discussed briefly.

Area

Layout is especially challenging for this project since the analog transmitter circuit is designed for a digital sea-of-gates structure. For analog circuits, it is usually the case that consumed area is not very important, or not as important as fulfilling other important requirements such as providing for parasitic resistances or capacitances at points which these unwanted effects would degrade circuit performance.

It is however important to optimize for area, after taking some of the other more important factors into account, because the used chip is meant to provide silicon for an entire RFID transciever upon completion. The transmitter should therefore consume an area as small as possible to allow for the implementation of the rest of the device. For this work specifically it is only important to be able to fit the four test structures on the same chip and this is where the area considerations are taken into account.

Symmetry

The first point taken into consideration is layout symmetry, this is because the circuit outputs a differential sine-wave and therefore symmetry is important to avoid signal *skewing* in the differential output values. Signal skewing could occur when the signal path of one of the differential outputs has a higher delay, resulting in a phase difference greater than 180°. This will therefore cause additional distortion in the output signal upon subtraction, if not handled.

Isolation

Four transmitters are implemented on the same chip, it is needless to say that if they all operated at the same time; the output signals will interfere greatly making measurements on the structures unreliable. Two remedies could be applied to overcome interference, the first being to place a metal wire around each structure hence isolating it better in terms of interfering signals [20]. The other simpler solution, which is used in the actual implemented chip, is to simply isolate the power inputs of each oscillator, so that if one oscillator is working, the others are switched off.

Floorplanning

In deciding the placement of the four test-structures it is first priority to have the RF output pads as close as possible to the actual output of the circuits. This is done to avoid loading the circuit with the parasitic resistances and capacitances that could result from using much wiring at the output. It can be seen in fig.

9.12 that the output pads are all at the same side, and all at the bottom of the chip, with minimum distance from the circuits.

For the ring oscillators it is required to place RC filters to avoid noise on the tuning inputs and supply rail. To take this into account, the supply rail is designed to be very long in order to have space enough to place MOS-capacitors between the V_{DD} and V_{SS} supply rail. For the RC filters, not much could be done except routing of the wires appropriately because the location of the capacitors and resistors used are fixed in the analog section of the chip.

Matching and Device Splitting

The transistors used for the cross-coupled transistor pair are required to be well matched to avoid asymmetry in the oscillator structure. To achieve this, the lower structure in fig. 9.2 is used. This structure greatly reduces any mismatch since the transistors are *spread* across the two NMOS and PMOS lines. To elaborate, each transistor consists of 12 fingers for the PMOS case, instead of having the 12 fingers of each transistor in the vicinity of each other, the fingers of the 2 transistors in the cross-coupled pair are placed in alternating fashion, so that 2 fingers from each transistor are placed alternating with the other. When this is done, the mismatch that occurs in one of the transistors will be the same in the other one therefore cancelling the effect of any mismatches. This is further clarified in the figure.

Wire widths

Wire widths in analog layout are important since there is a limit on how much current can flow in a unit width of the wire, a larger current may cause overheating in the wire leading to damage, or a lot of loss in voltage may occur due to the resistance of a narrow wire for example. The general rule of thumb used in this work is to have 1 mA per 1 micron width of the wire for the upper metal layer. Such a value is extracted after taking into consideration the resistivity of the used metal, and the acceptable voltage drop across a certain metal connection.

Parasitics

Parasitic losses in form of substrate capacitances or resistance are present at each node in any circuit, the trick is to try and reduce the parasitics in the circuit nodes in which they affect the circuit operation. In the case of oscillators it is very important to reduce the resistance in the branch of the inductor because any series resistance would degrade the inductor Q in proportion. It is also of importance to reduce the resistance on the oscillation nodes for the same reason. It is however always the case that a tradeoff is made: to reduce the resistance, the

wire width is increased which in turn increases the unwanted capacitance there, but the capacitance only reduces the oscillator frequency therefore redesign of the originally used capacitor values can be done to overcome this simply.
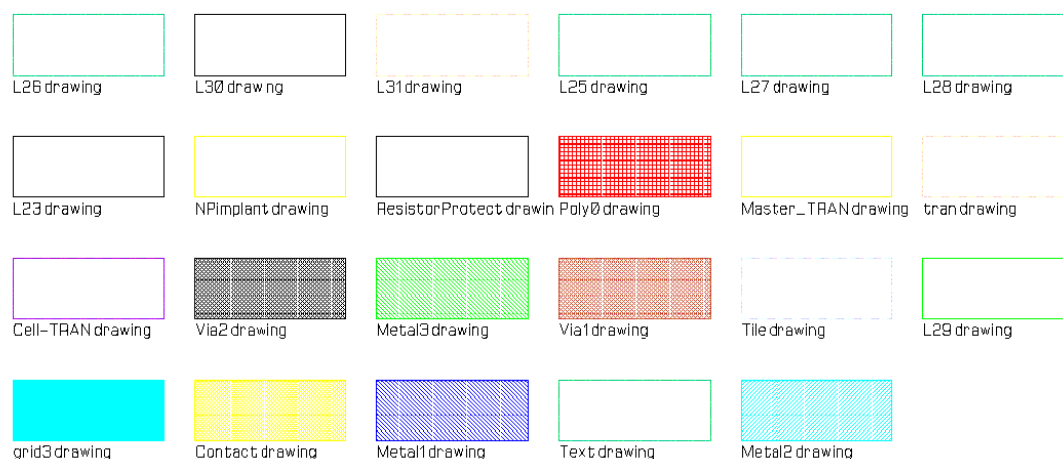
Figure 9.1: Color key used in layout.

9.2 Cross-Coupled Oscillator Layout

The most important part is the transistor cross-coupled pair. During their layout their placement is chosen to be as close as possible to the inductor. This is done to ensure the most effective compensation of the inductor losses, since the cross-coupled transistors are responsible for cancelling out the parasitic resistance of the inductor as discussed in chapter. 4.

Another issue is symmetry; this is required in all oscillators but is traded-off here for matching. As mentioned above, matching can be reduced by spreading the transistor over many fingers widely spaced from each other. Consider fig. 9.2 where two different implementations of the cross-coupled pair is shown. In the first implementation, all the fingers for each transistor are placed together in the same area. In the second implementation, however, it can be observed how the PMOS transistor fingers are interchanged between the layout structure: The PMOS row consists of alternating fingers, one from a PMOS transistor then the next from the other, and so on. This assures that overall matching becomes good between the transistors since any offsets or changes are bound to be cancelled out by averaging their effect which is achieved through the shown structure [20].
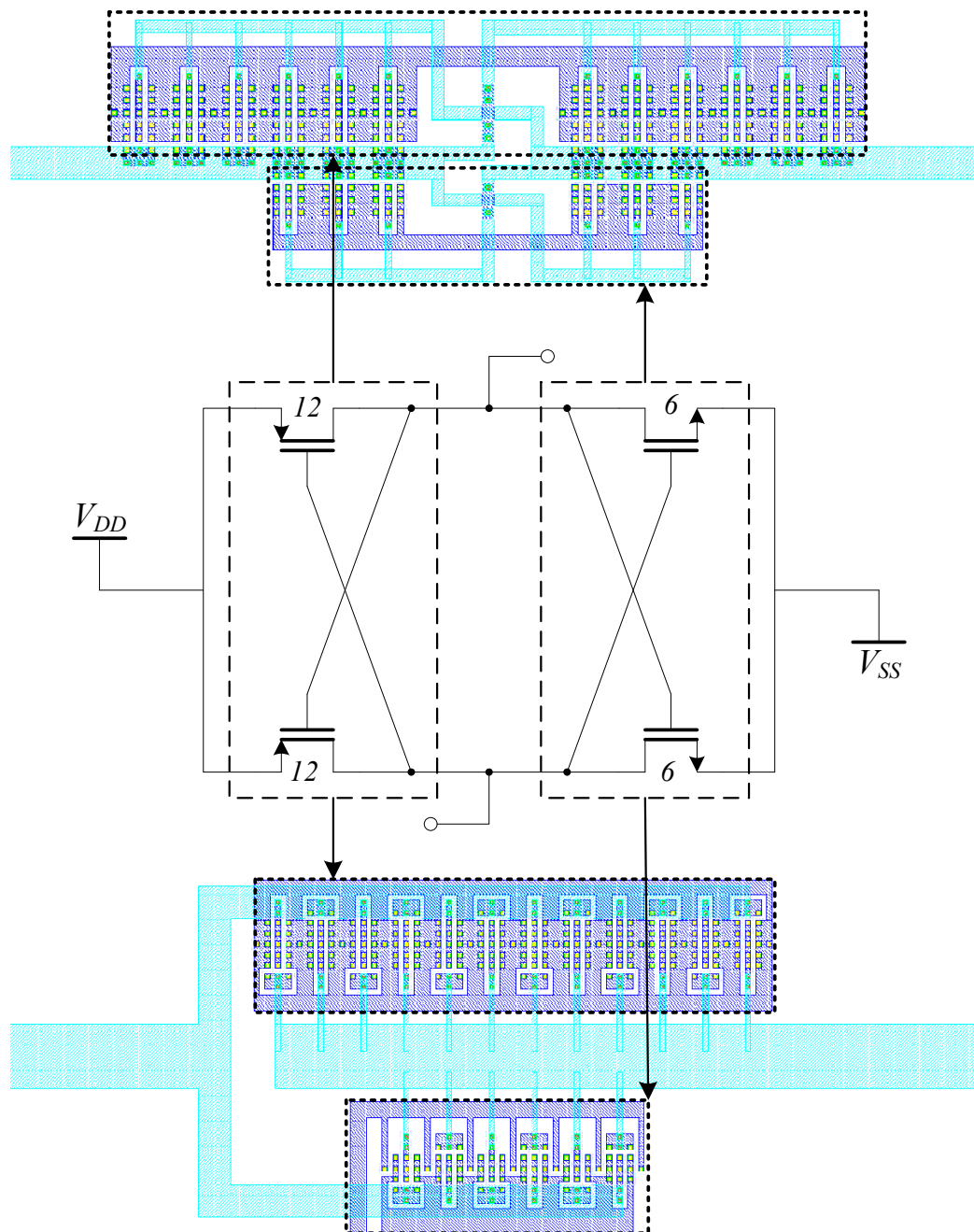
Figure 9.2: Layout for two different implementations of the cross-coupled pair.

Layout of varactors is designed to be symmetric as well, as can be seen from fig. 9.3. Varactors are designed to very large sizes; up to 400 fingers, note that the shown example only has 20 fingers. In designing the large varactors it is important to not have a large wire length between the control input and the other terminal of the varactor so that all of the fingers would have a uniform voltage drop. The FSK modulator is shown in fig. 9.4. It consists of a small varactor and therefore the same considerations applied to varactor design are done here.

Layout of the ASK modulation stage and driver is shown in fig. 9.5, the figure shows the layout and the schematics with corresponding labels on each. The signal path in this structure is assured to be the same length (for each of the differential paths), and the design is made as symmetric as possible. Power is fed through two main thick wires; V_{DD} from the bottom and V_{SS} at the top.

Fig. 9.6 shows the layout of the entire cross-coupled oscillator-based transmitter, the various components are labeled on the figure. It can be immediately noticed that the layout is symmetrical and the two differential signals have the same lengths, overall, and in each section. The monolithic inductor occupies a large area as it as can be seen from the layout. The next largest component is the capacitors and the varactors, it is therefore the passive components in the LC resonator that occupied most of the circuit's area.
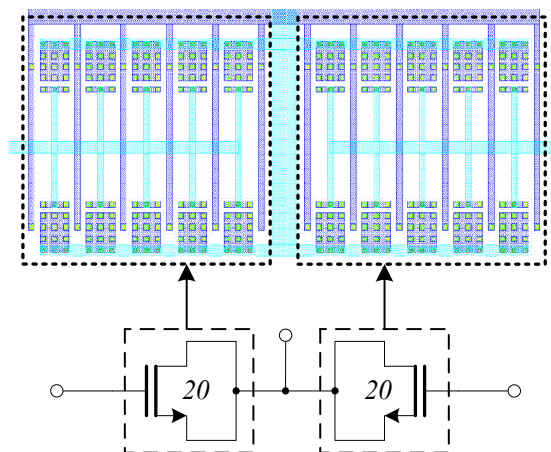
Figure 9.3: Layout of a multi-finger MOS varactor.

Since there are only two metal layers available, the power inputs had to be well thought out in order to arrive at an area efficient yet effective method for power inputs. Due to the lack of metal layers, a power grid is difficult to implement, it is therefore the design choice to create power rings; one for V_{DD} and the other for V_{SS}, this can be seen clearly on the figure. The placement of the power rings
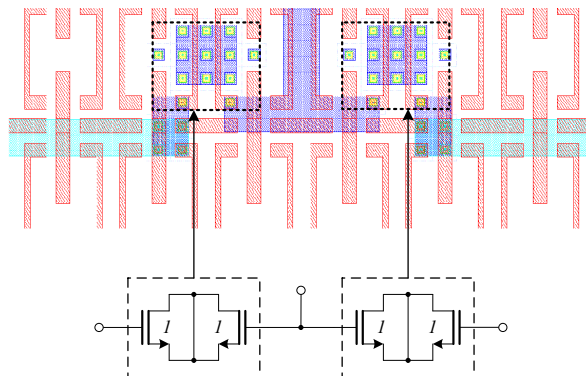
Figure 9.4: Layout of the FSK modulation varactor.

is done such that the edges are in the vicinity of the devices that required them most, then connections are taken from them with cross-overs when necessary using the other metal layer. Note that the power rings are implemented in the less conductive lower metal layer since the better higher metal layer is used for the signal path.

9.3 Differential Ring Oscillator Layout

Since the transistors are organized in form of NMOS and PMOS transistor rows, one inverter stage is implemented as shown in fig. 9.7 with all the n-channel transistors next to each other, then the p-channel transistors placed above them. This is also done because the connection between the current sources and the transistors is required to be as small as possible to avoid voltage drop on that connection which would disturb bias conditions. Another advantage in doing so as well is that the PMOS transistors, when moved sufficiently further from the NMOS section, allow for connecting the signal path in an efficient, low-delay path.

It can be seen now in fig. 9.8 how each inverter is placed: The inverters are placed one after the other in alternating inverted form such that two of the five inverters are placed *upside down*. This allows connections to be made between the inverters in the most area efficient way. Not to mention that the signal path is now as small as possible, meaning that the delay between each inverter is minimized, resulting in a faster ring oscillator chain. In addition, the wire differential paths have overall equal lengths.

Power is input to this ring oscillator also in form of two power rings, corresponding to V_{DD} and V_{SS}, this is done similarly to the cross-coupled oscillator since it is also found suitable here. The output stages, comprising of the ASK
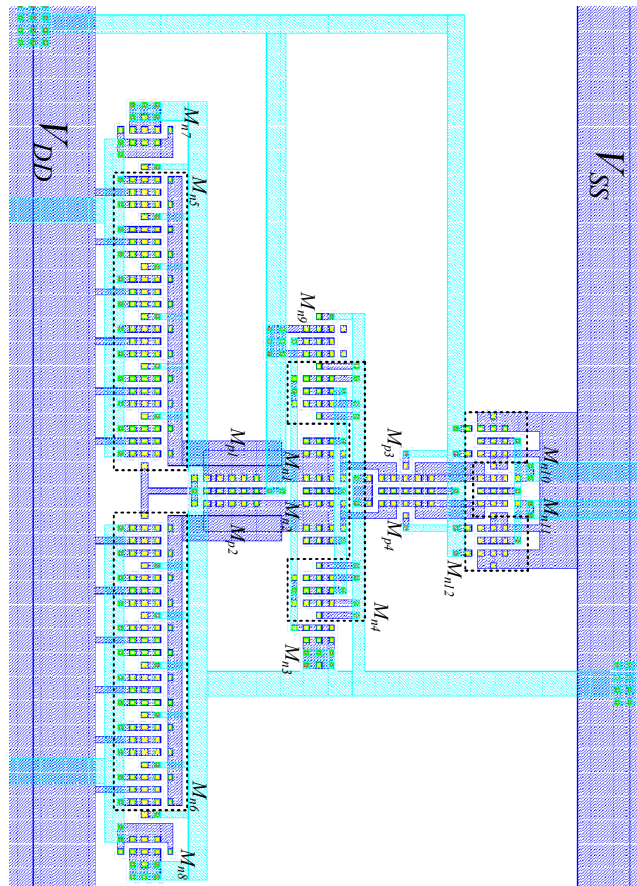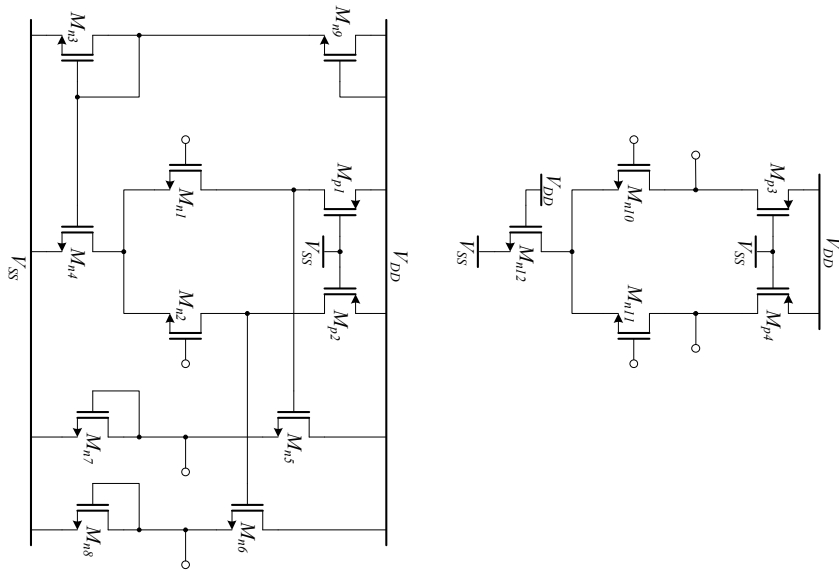
Figure 9.5: Layout of the ASK driver.
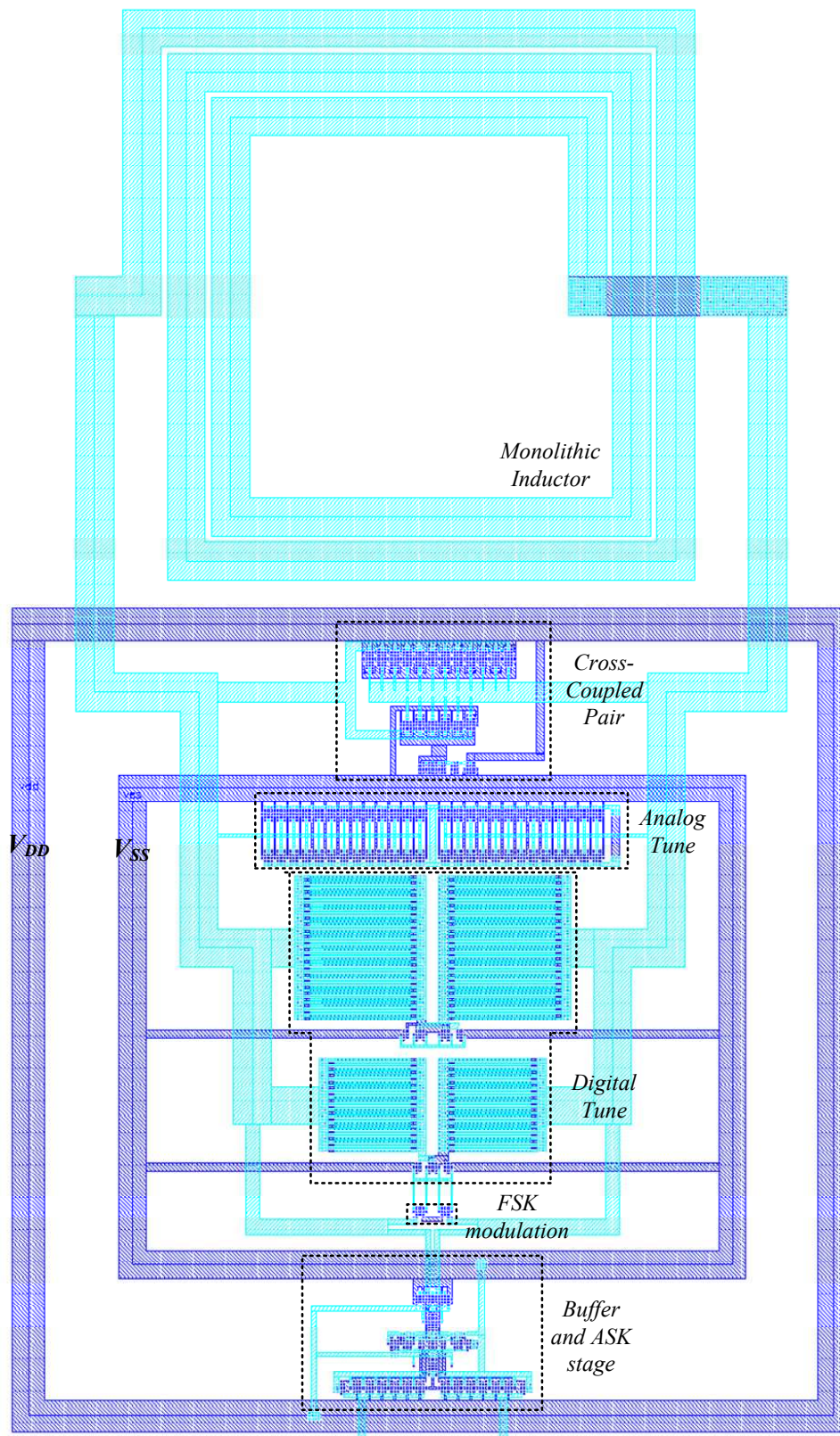
Figure 9.6: Layout of the 2.4 GHz cross-coupled oscillator.
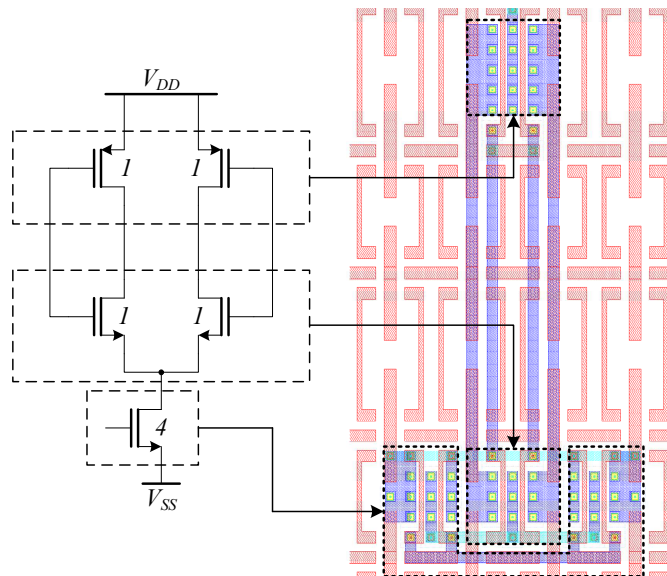
Figure 9.7: Layout of 1 inverter from the differential ring oscillator.

modulation stages and buffer and driver, are also implemented in a very similar way to the one in the cross-coupled oscillator. This is because it is the same structure, only with different sizes of some of the transistors.

9.4 Single-ended Ring Oscillator Layout

Ring oscillators are very simple circuits in design, and in layout as well. Since this circuit has s single-ended topology, symmetry is not an issue, focusing the design mainly on area optimization. One CMOS inverter stage is shown in fig. 9.9. Its construction is very simple; using only one of the two metal layers, the drains and gates of the transistors are connected together to form one inverter.

It can be seen from fig. 9.10 how area optimization is taken into account: the complete silicon area used in the ring oscillator is $0.04mm^2$. Two rows of n-channel transistors are utilized and only one from the p-channel transistors. The connection between each inverter is very short except for the final feedback wire, it is quite long since it is required to connect the end of the chain to the very first one. For this connection it is important to extract and simulate the parasitic resistance and capacitance, and after doing so, it is found that this long connection had only a small effect on the oscillator's performance, and that it is more important to optimize for area.

The CMOS driver and buffer sub-circuits are implemented in the same way as the inverters as described earlier. Furthermore they are simply placed following
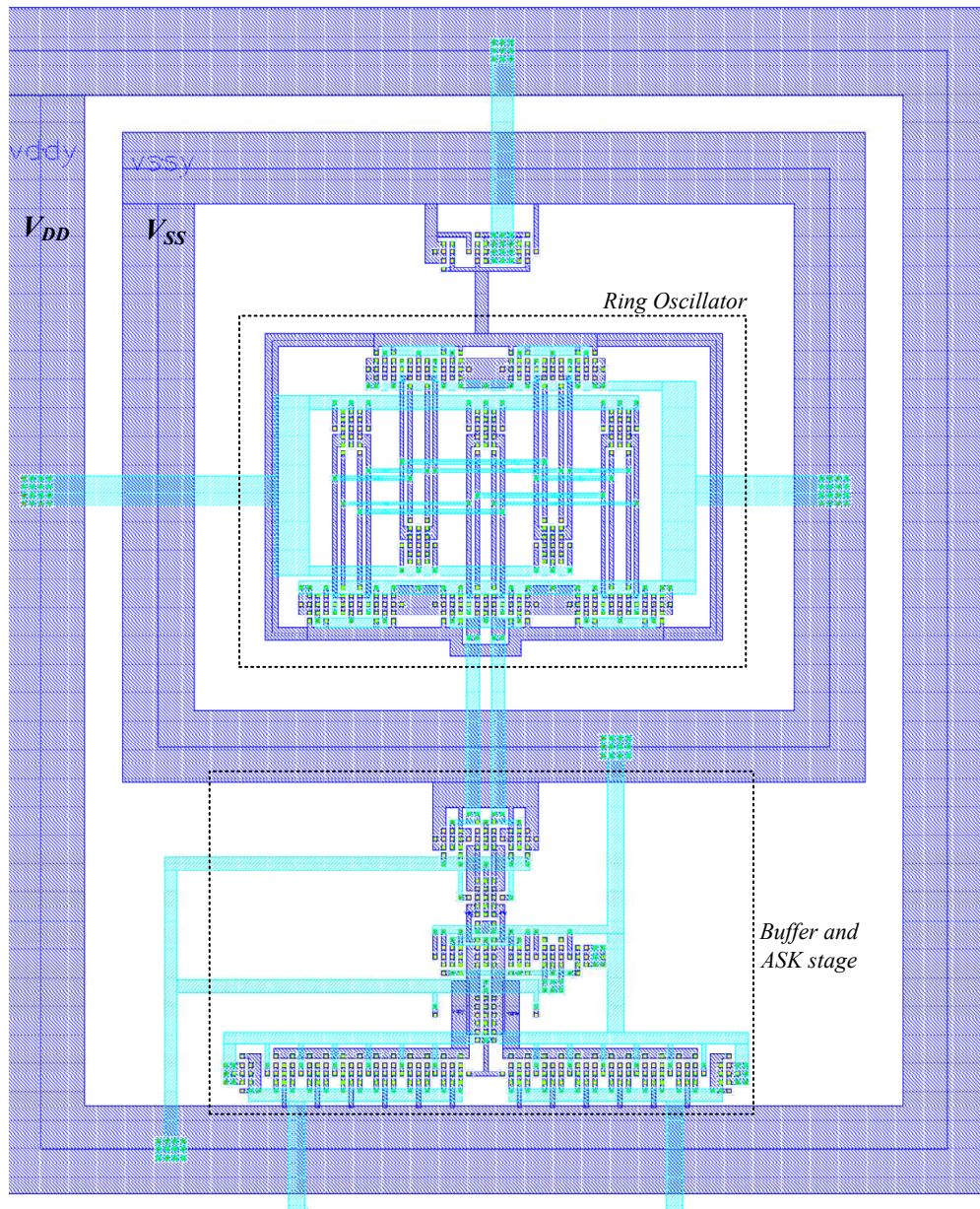
Figure 9.8: Layout of the differential ring oscillator.

the oscillator chain to optimize for area as well. What remains to complete the transmitter is the various current sources which are placed next to one another in a separate row of n-channel transistors, connections are then made to the inverters. It is worthy to note that in the differential ring oscillator it is more important to have this connection as short as possible because the tail current is more critical in differential implementations but in the case of the single-ended implementation shown here, it will at most result in a small offset in the bias current range.

As for the power inputs to the oscillator, due to the simplicity of the presented design, it is sufficient to have two thick wires: one for V_{DD} north of the circuit and the other for V_{SS} at the south. Later on, the wire for V_{SS} is completed as a ring as well, so that routing to the pad connections is easier but not for the sake of the oscillator itself.
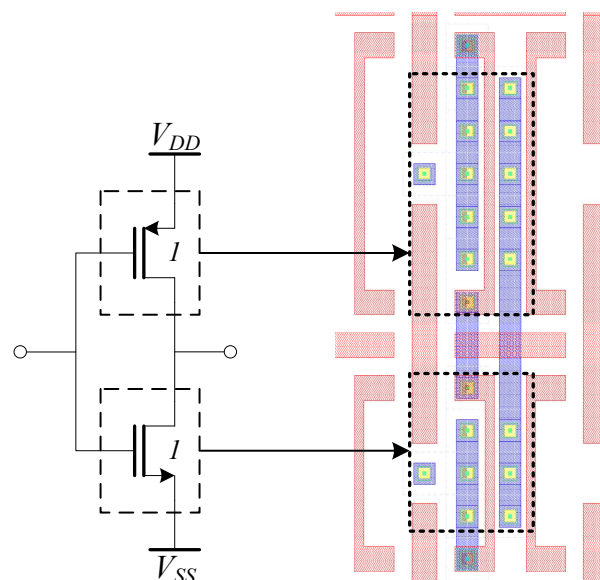
Figure 9.9: Layout of 1 inverter from the single-ended ring oscillator.

9.5 Complete Chip Layout

In designing the transmitter circuits it is of importance to follow the analog design rules and to design for maximum efficiency as well as smallest area without degrading the circuit function. Now, in the layout of the entire test-chip another constraint comes into play, it is essential to facilitate testing and measurements of
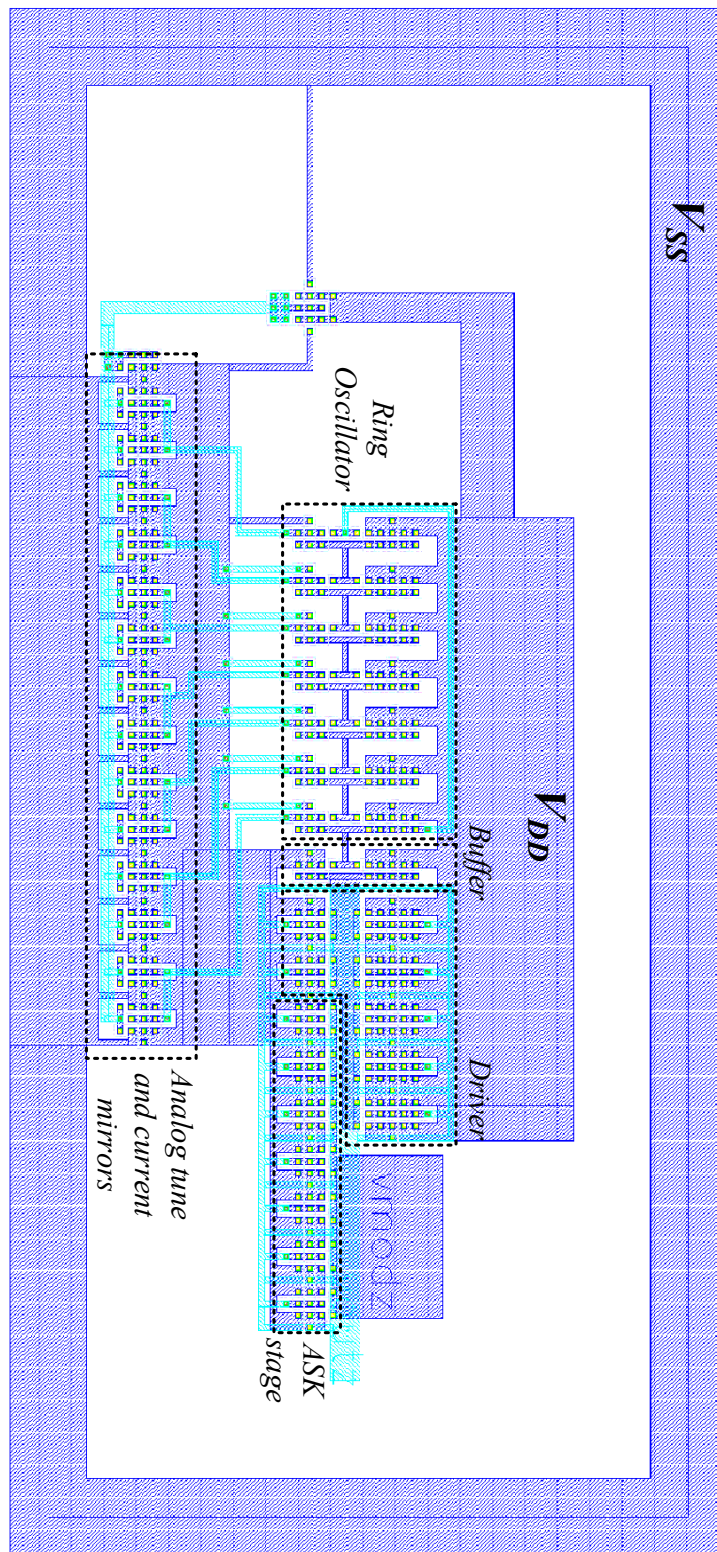
Figure 9.10: Layout of the single-ended ring oscillator.

the structures since this is the purpose that the chip must fulfill. In addition, the connections to the inputs and outputs had to be carefully designed to conform to the type of input or output. This, and some other layout design points are discussed in this section.

9.5.1   Floorplanning

In choosing where to place the circuits designed, the pad connections have to be taken into consideration; the first and most important condition imposed on the design is to have a minimum wire length for the RF outputs. This is done to reduce losses and be able to measure the output signal as it is, without attenuation. This is indeed taken into account, it can be seen from fig. 9.11 that the circuits are situated south of the chip and all the outputs are taken from below, with minimum distance from the circuits to the pads.

The wire connections, especially those used for V_{DD} and V_{SS} had to be sized appropriately to support the current flowing through them. The general rule of $1\mu m$ per 1 mA for metal 2 layer (and twice that value for metal 1) is used, this is calculated by taking into account the conductivity of the metal layer [20] and the acceptable voltage drop across one connection. As another rule of thumb, the voltage drop on any wire is chosen not to exceed 100mV.

9.5.2   Pads

The placement of the pads is done such that inputs/outputs of similar types are placed at the same side of the chip. For example, note how all the GSSG outputs are south of the chip, and that PGSSGP are all at the top while the PGSSSP are at the sides. It is not directly observable but this is important and has one main and very important advantage: this facilitates testing since it will allow switching from measuring one circuit to the next simply by raising the probes and moving the chip, without the need of disconnecting and reconnecting the probes, or reprogramming them to different inputs even, which could be a tedious and maybe even an erroneous process.

The pads used for the inputs comprised of two metal layers with connections between the two, the use of two metal layers increased the pad capacitance which is desired for DC or tune inputs since it helps in noise blocking. As for the RF output pads, the lower less conductive metal layer is removed so that only a single-metal-layer pad, with only the more highly conductive metal, is used for this purpose. It is critical to do this modification to reduce the capacitive loading on these pads which would deteriorate the signal measured from it. The pads in this design were standard to the chip used having $108\mu m$ pitch and a size of $100\mu m \times 100\mu m$.
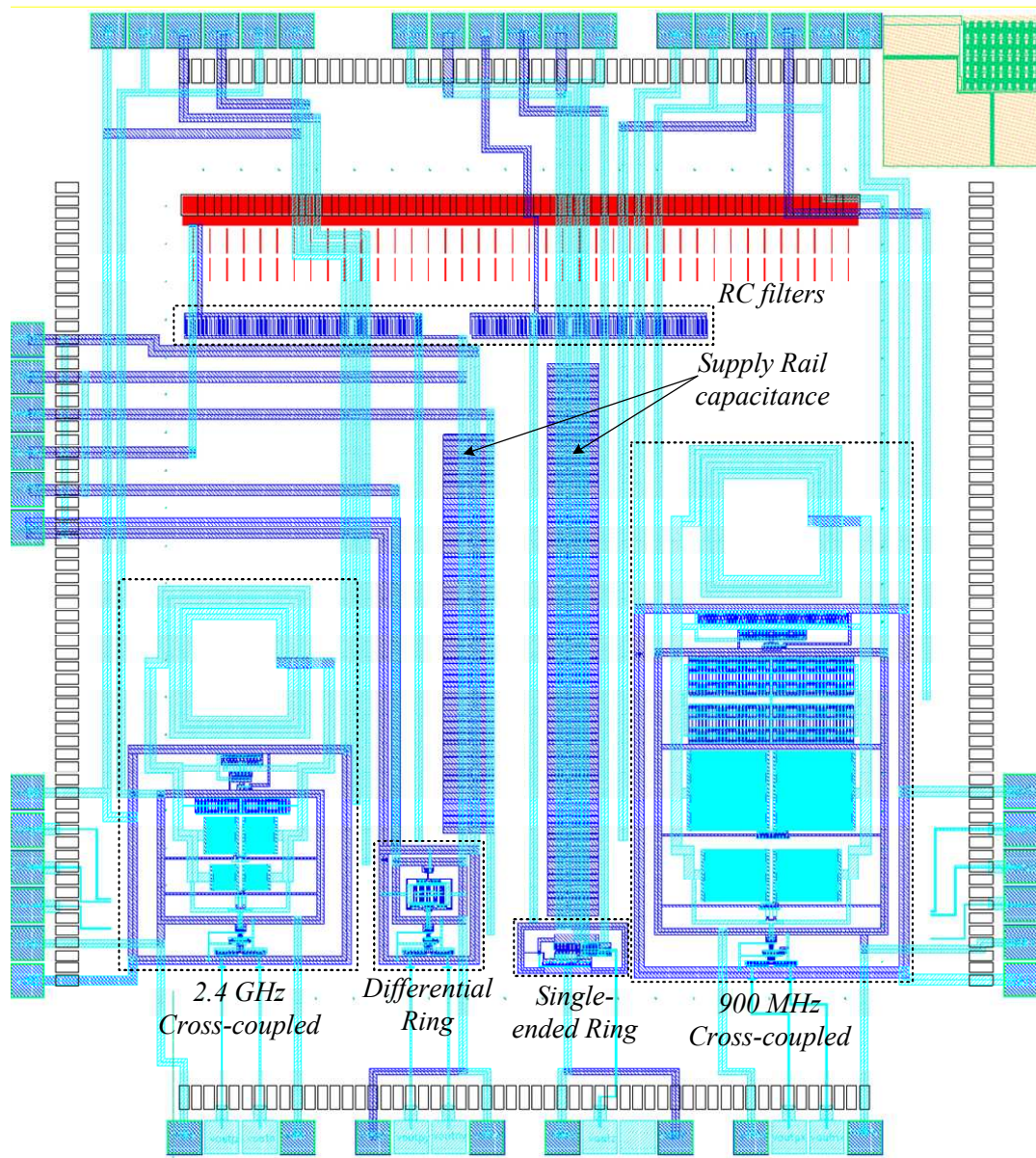
Figure 9.11: Layout of the completed Promikron testchip.

If a closer look is taken at the connection between the pad and the wire connections, it can be seen that when the wire is thin: a metal block, almost one third the size of the pad, is placed as a transition from the wire to the pads. By placing this metal block, the thin wire is protected from being broken, which could occur due to stresses from the measurement probes on the pads.
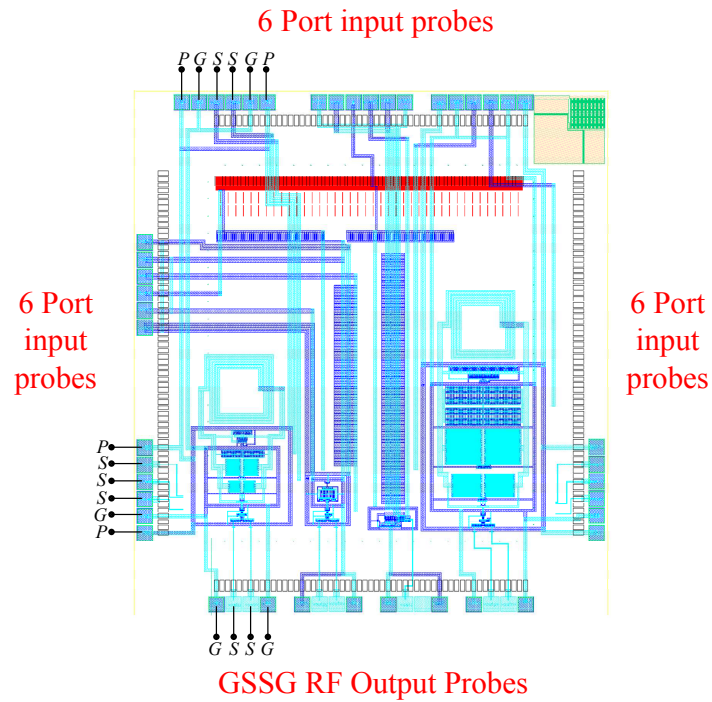
Figure 9.12: Example pad connection for the 2.4 GHz cross-coupled oscillator.

Chapter 10

Summary and Future Work

Work in this project was mainly about testing a transmitter circuit using a new technology which was principally used for digital integrated circuits before. The design process was therefore started by simulation, measurements and modeling of the various passive and active structures that were to be used in the circuit. After having established a reliable simulation model for each of the circuit components, circuit design was started. In designing the transmitter circuits it was important to keep low complexity since this was only a first prototype.

To test the technology effectively, two oscillator topologies were implemented, each having a different principle of operation: ring oscillators and cross-coupled oscillators. They were also designed such that different frequencies of operation were covered.

In table 10.1, a summary of the simulation results is presented. It is easily observed that the ring oscillators are superior in terms of area, power consumption and tuning range as well. The cross-coupled oscillators however, show much better spectral purity and tuning linearity, not to mention that they operate at higher frequencies than their ring-oscillator counterparts.

Future Work

After creating the prototypes, much work is still needed to arrive at a final version of the RFID transmitter. Pending fabrication comes the first step: testing and measurements of the VCO structures which will lead to the choice of the suitable VCO structure for use. A next step will involve investigation of the possibility of integrating the VCO in a phase locked loop (PLL), which would be required to lock on to the operating frequency.

The phase locked loop will have many challenges: creating the frequency reference being the toughest because there is no integrated crystal for the used technology. It is therefore needed to explore whether it would be achievable to

	Feature	Cross 2.45GHz	Cross 900MHz	Diff. Ring	Single Ring
-	Total area	$0.57mm^2$	$0.89mm^2$	$0.07mm^2$	$0.04mm^2$
# trans.	VCO	58	148	76	45
	Buffer & Driver	36	34	42	30
	Total	94	183	118	75
Power	VCO	23 mW	60 mW	17 mW	7 mW
	Buffer & Driver	34 mW	34mW	36 mW	45 mW
	Complete Circuit	57 mW	94 mW	53 mW	53 mW
	50Ω Loaded	163 mW	196 mW	180 mW	76 mW
Tuning	Tuning Ratio	39%	41%	-	-
	Tuning Range	2.0-2.95 GHz	730-1100 MHZ	0-1.2 GHz	0-0.9 GHz
Output	Unloaded V_{pp}	2.5 V	3 V	5 V	5 V
	50Ω Loaded V_{pp}	1 V	1.4 V	2 V	1.4 V
-	Tail current	5 mA	15 mA	0 - 4 mA	0 - 4 mA
-	Modulation	FSK +/- 300kHz	FSK +/- 50kHz	ASK 1:0.3	ASK 1:0.3
-	K_{VCO}	125 MHz/V	58 MHz/V	325MHz/mA	210MHz/mA

Table 10.1: Summary of simulation Results

lock on to an external frequency, possibly from the RFID reader.

Power input is also an issue of discussion for future work. One possibility is to have the power transmitted wirelessly from the RFID reader as well. The frequency (possibly 13.5 MHz) of this "power wave" would also be used as the reference frequency for the PLL.

Another issue of discussion which was not investigated and left for future work was to take a new approach to the RFID system by having an ultra-wide band transmitter working at low power. This would eliminate the need for a PLL, but transmitting power and operating range require investigation so as not to interfere with other frequency bands.

Appendix A

Design Values

Design values for the designed circuits are summarized here in tables A.2 and A.3. The tables show the number of fingers used for each transistor or the equivalent design value for a passive element.

The transistor model used was provided by vendor *IMS-CHIPS*. The transistor parameters used were as shown in the following table A.1 for the n-channel and p-channel transistors.

	Transistors	
	n-channel	p-channel
Width (μm)	7.6	12.4
Length (μm)	0.5	0.55
NRS	1/7.6	1/12.4
NRD	1/7.6	1/12.4
AS	$34.02p \times 0.6 \times 0.6$	$31.93p \times 0.6 \times 0.6$
PS	$30.599\mu \times 0.6$	$23.700\mu \times 0.6$
AD	$20.16p \times 0.6 \times 0.6$	$54.589p \times 0.6 \times 0.6$
PD	$15.799\mu \times 0.6$	$46.500\mu \times 0.6$

Table A.1: Transistors parameters used.

Transmitter	Block	figure	transistor(s)	# of fingers
Cross-coupled 2.4 GHz	Oscillator	fig. 6.7	M_{n1}, M_{n2}	6
			M_{n3}	1
			M_{n4}	4
			M_{n5}	2
			V_{n1}, V_{n2}	52
			$V_{n(3-6)}$	1
			C_{fixed}	zero
			C	0.3 pF
			L	4.5 nH
	Output Stage	fig. 6.8	M_{n1}, M_{n2}	1
			M_{n3}	4
			M_{n4}, M_{n5}	2
			M_{n6}	4
			M_{n7}	1
			M_{n8}	2
			M_{n9}, M_{n11}	12
			M_{n10}, M_{n12}	1
			M_{p1}, M_{p2}	1
			M_{p3}, M_{p4}	1
Cross-coupled 869 MHz	Oscillator	fig. 6.7	M_{n1}, M_{n2}	20
			M_{p1}, M_{p2}	44
			M_{n3}	1
			M_{n4}	9
			M_{n5}	2
			V_{n1}, V_{n2}	384
			$V_{n(3-6)}$	1
			C_{fixed}	2 pF
			C	2.5 pF
			L	4.5 nH
	Output Stage	fig. 6.8	M_{n1}, M_{n2}	1
			M_{n3}	4
			M_{n4}, M_{n5}	2
			M_{n6}	4
			M_{n7}	1
			M_{n8}	2
			M_{n9}, M_{n11}	12
			M_{n10}, M_{n12}	1
			M_{p1}, M_{p2}	1
			M_{p3}, M_{p4}	1

Table A.2: Cross-coupled oscillators design values.

Transmitter	Block	figure	transistor(s)	# of fingers
Differential Ring Oscillator	Oscillator	fig. 6.9	M_{n1}, M_{n2}	6
			M_{p1}, M_{p2}	1
	Current Source	fig. 6.10	M_{n1}	2
			M_{n2}	1
			$M_{n(3-5)}$	4
	Output Stage	fig. 6.8	M_{n1}, M_{n2}	1
			M_{n3}	4
			M_{n4}, M_{n5}	1
			M_{n6}	4
			M_{n7}	1
			M_{n8}	2
			M_{n9}, M_{n11}	12
			M_{n10}, M_{n12}	1
			M_{p1}, M_{p2}	1
			M_{p3}, M_{p4}	1
Single-ended Ring Oscillator	Oscillator	fig. 6.11	$M_{n(1-7)}$	1
			$M_{n(8-14)}$	4
			M_{n15}	1
			M_{n16}	2
			$M_{p(1-7)}$	1
	Output Stage	fig. 6.12	M_{n1}	1
			M_{n2}	4
			M_{n3}	14
			M_{p1}	1
			M_{p2}	10

Table A.3: Ring oscillators design values.

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